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Design and fabrication of lateral high power devices for power integrated circuits applications

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Design and Fabrication of Lateral High Power Devices for Power Integrated Circuits Applications

by

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Abstract

The incorporation of high power devices on the same chip as that of the circuitry controlling the high power device has been shown to provide several major advantages over discrete and multichip module designs. The major focus of this work is the development of lateral high power devices that are compatible with R.I.T.'s low power CMOS process. The thrust of this study is to evaluate the feasibility of fabricating Power Integrated Circuits at R.I.T's semiconductor die manufacturing laboratory.

As part of the development, several types of high power devices were investigated and the Power MOSFET and IGBT were chosen to be fabricated. The Power MOSFET and IGBT were chosen because they were the least complicated and would provide the greatest probability of functionality. The bulk of the work involved studying the effect of the field plate overlap on the breakdown voltage and the on state resistance. The basic process needed to fabricate the power device was designed and a SUPREM 4 simulation has been generated. The designed process produced a power MOSFET with a breakdown voltage of 50 volts and an operating current of nearly 0.5 amps with an on state resistance of 35Ω, while maintaining the standard CMOS operating characteristics for the low power devices. The results are discussed and recommendation for future work at R.I.T. are provided.

List of Figures

List of Tables

LIST OF SYMBOLS

RIT	Rochester Institute of Technology
IC	Integrated Circuit
CMOS	Complimentary Metal Oxide Semiconductor Transistor
MOSFET	Metal Oxide Semiconductor
IGBT	Insulated Gate Bipolar Transistor
V	Volts
A	Amps
Ω	Ohms
PIC	Power Integrated Circuit
VLSI	Very Large Scale Integration
MOS	Metal Oxide Semiconductor Transistor
NMOS	N Channel Metal Oxide Semiconductor Transistor
PMOS	P Channel Metal Oxide Semiconductor Transistor
DMOS	Diffused Metal Oxide Semiconductor Transistor
Ids	Current from drain to source
Vgs	Voltage from gate to source
Vds	Voltage from drain to source
BJT	Bipolar Junction Transistor
Ic	Collector current
Ib	Base current
Vce	Voltage from collector to emitter
μm	Micro-meter
Vt	Threshold voltage
NFET	N Channel Field Effect Transistor
IBT	Insulated Base Transistor

LEST	Lateral Emitter Switch Transistor
VLSI	Very Large Scale Integration
ψs	Silicon Potential
Φf	Fermi Potential
Φms	Work Function
kT/q	Thermal Voltage
k	Boltzmann's Constant
T	Temperature
q	Charge on a electron
Na	Acceptor atom concentration
ni	Intrinsic carrier concentration
ψox	Oxide potential
Q	Total Charge
Qb	Bulk Charge
Qi	Intrinsic charge
Qss	Interface trap charge
Cox'	Oxide capacitance per area
εo	Permitivity of free space
εox	Permitivity of oxide
εs	Permitivity of silicon
Xox	Oxide thickness
Jn	Electron current density
μn	Electron mobility
E	Electric field
Jdrift	Current density due to drift
Jdiff	Current density due to diffusion
W	Width

L	Length
GTO	Gate Turn Off Transistor
a	Anode
k	Cathode
G	Gate
D	Drain
S	Source
b	Bulk
Vh	Holding Voltage
Vbo	Break over voltage
Ig	Gate current
BV	Breakdown voltage
Xd	Depletion region length
Xp	Depletion length in P region
Xi	Depletion length in little doped region
Xn	Depletion length in N region
Nd	Concentration of donor atoms
Ni	Concentration of donor atoms in litle doped region
Φi	Built-in potential
Va	Applied Voltage
R	Resistance
C	Capacitance
LV	Low Voltage
HV	High Voltage
epi	Epitaxual
Sub	Substrate
SiO2	Silicon Oxide

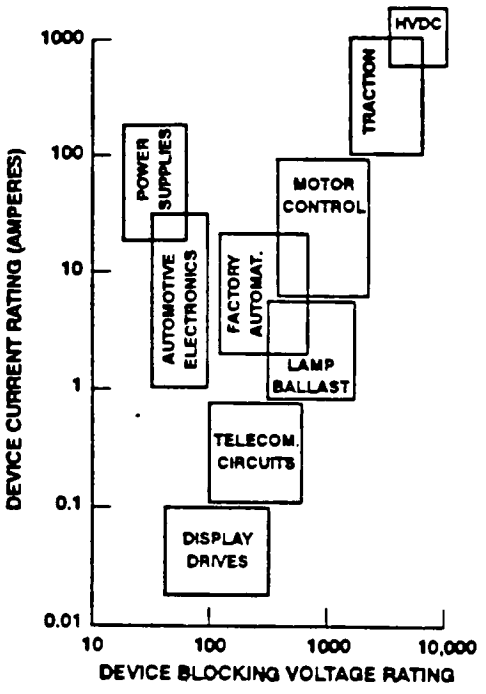
EEPROM	Electrically Erasable Programmable Read Only Memory
FOX	Field Oxide
FPO - -	Field Plate Overlap
LTO	Low Temperature Oxide
SOG	Spin On Glass
CVD	Chemical Vapor Deposition
Al	Aluminum
tox	Oxide thickness
Xj	Junction depth
PWR	Power
cm	Centi-meter
H2O2	Hydrogen peroxide
NaOH	Ammonia hydroxide
HCl	Hydrochloric acid
DI	De-Ionized
O2	Oxygen
N2	Nitrogen
C	Celsius
min	minute
å	Angstrom
KeV	Kilo-electron volt
AMU	Atomic Mass Unit
H2	Hydrogen
HF	Hydrofluoric acid
Temp	Temperature
RIE	Reactive Ion Etch

Table of Contents

1. Introduction

Signal processing has been a focal point for a majority of the activity in the development of I.C.s. Both analog and digital forms have been developed extensively. Advancements in VLSI technology have surpassed many of the initial expectations in a surprisingly short amount of time. During the mid 1980's, it became increasingly apparent that the application of solid state technology to systems was being curtailed by the lack of low cost, compact, highly reliable power electronics. The rectification of this single sided approach has become a dominant force in the up grade of power devices.

With these new developments, several power devices can be seen to have similar forms to their low voltage counter parts. From this, the advantages of developing design, processing and packaging techniques that allow the integration of high voltage power device structures with low voltage control circuitry on a single silicon chip has become apparent. The advantages range from reduced size and power consumption to increased control and reduce parasitic effects. These Power Integrated Circuits (PIC) have applications in automotive electronics, power supplies, display drives, telecommunications, motor control and ad isolation techniques improve, look to move into other areas. Fig 1.1 shows a graph relating the application to both the blocking voltage and current rating required. Current PIC lie predominantly between 500 volts blocking and 50 amps conducting but look to expand as improvements are made.



Plot of current ratings vs. blocking voltage ratings for PIC applications

Fig. 1.1

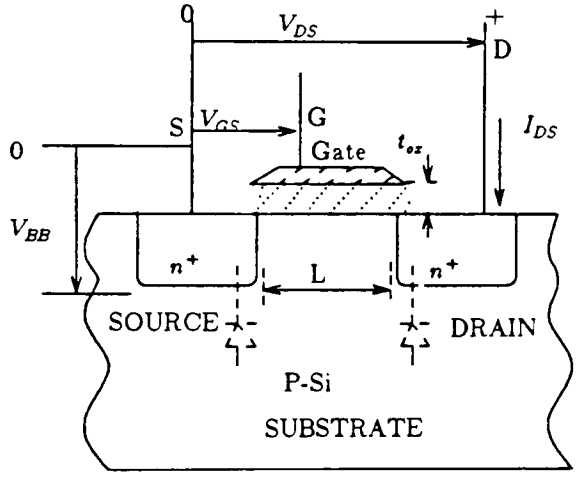
PIC technology is one of the most advanced and complex structures being produced in electronics today. These circuits can be found to incorporate power and control circuits utilizing BiCMOS or Bipolar and CMOS technologies and power DMOS or IGBTs.

An overview of both high and low power devices is presented to provide a basic relationship between the two. Details of the I.C. compatible high power devices and their incorporation in I.C.s are then presented. The following sections describe the procedures used in the design of the high power P-well CMOS compatible power devices and the development of a fabrication technology. The low and high power devices are characterized from a static viewpoint. The electrical results are presented and discussed Conclusions on the practicality of the fabrication process and design are drawn.

2. Device Background

2.1 Low Power Devices

The purpose of this section is to review the main characteristics of a MOS transistor so that a common point of reference can be achieved for future comparisons of the high and low powered devices. Fig 2.1 shows a diagrammatic cross section of an NMOS transistor.



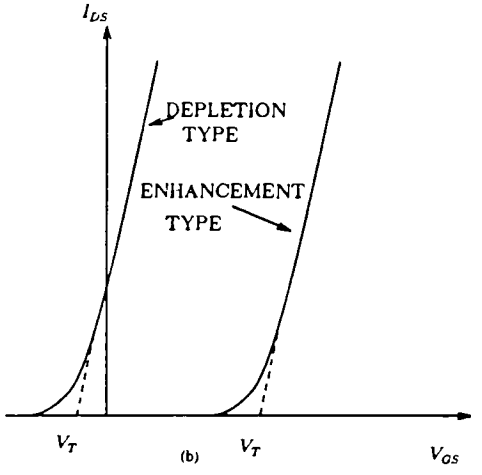
Diagrammatic cross section in an NMOS transistor showing parasitic diodes and terminal voltages

Fig 2.1

An applied positive voltage, Vds, allows electrons to flow from the source to the drain when a channel is present. A channel will form when Vgs is equal to or greater than the threshold voltage. The threshold voltage is the applied gate voltage which causes the silicon surface of the device to be at the onset of inversion, or when the surface potential, Ψs, is $2\Phi f$. Φf is defined as he potential between intrinsic and extrinsic silicon if the two were brought in contact and thermal equilibrium were established.

$$\Phi f = (kT/q) \ln(Na/ni) \qquad \text{Eq 2.1.1}$$

Where kT/q is 0.026 v at 300 K and is known as the thermal voltage, Na is the bulk substrate concentration and ni is the intrinsic carrier concentration of silicon, approximatly 1.45 cm-3 at 300 K. A plot of the current from drain to source, Ids, verses the voltage from gate to source, Vgs, is shown in Fig 2.2 and the threshold voltage, Vt, is noted.



Ids vs. Vgs curves for depletion and enhancement type transistors

Fig 2.2

The gate voltage can be expressed as

$$Vgs = \Psi ox + \Psi s \qquad \text{Eq 2.1.2}$$

Where Ψox is the potential drop across the oxide. Ψox may by expressed as

$$\Psi ox = -(Qb + Qi)/Cox' \qquad \text{Eq 2.1.3}$$

Cox' is the oxide capacitance per unit area, and is equal to

$$Cox' = \varepsilon o \, \varepsilon ox / Xox \qquad \text{Eq 2.1.4}$$

$$Q = [2\varepsilon sqN(2\Phi f)]^{\wedge}1/2$$

εo is the permittivity of free space, =8.85e-14 F/cm, εox is the permittivity of oxide, =4, and Xox is the oxide thickness. εs is the permittivity of silicon. If Qi = 0, then Vt can now be written ideally as

$$Vt = 2\Phi f + (1/Cox') [2\varepsilon sqN(2\Phi f)]^{\wedge}1/2 \qquad \text{Eq 2.1.5}$$

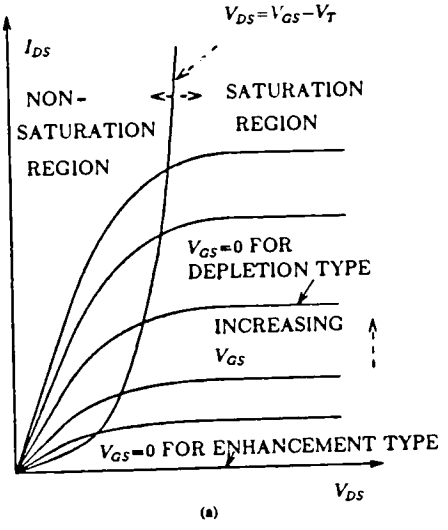
There are two non-idealities that should be considered. The first is the work function difference between the gate and the substrate, Φms. Φms is the change in gate voltage which is needed to maintain the same surface potential as if the gate and substrate were of the same material. The second is the effective interface charge, Qss. This is a composite of the oxide fixed charge, the oxide trapped charge and the interface trap charge. These non-idealities result in a threshold equation of:

$$Vt = \Phi ms + Qss/Cox' + 2\Phi f + (1/Cox') [2\mathcal{E}sqN(2\Phi f + Vsb)]^{1/2} \quad \text{Eq 2.1.6}$$

Vsb is the source to bulk voltage and causes a bulk effect, γ.

$$\gamma = (1/Cox') [2\mathcal{E}sqN(Vsb)]^{1/2} \quad \text{Eq 2.1.7}$$

When the transistor is conducting current, the Ids vs. Vds curve in Fig 2.3 can be expected:



Ids vs. Vds family of curves for NMOS transistors

Fig 2.3

To predict the current, Ids, the following approach is presented. The current density is

$$Jn = Jndrift + Jndiff \quad \text{Eq 2.1.8}$$

$$\Delta Jn = q\,\mu n\, n\, E + q\, Dn\, .\, n \quad \text{Eq 2.1.9}$$

assuming the diffusion current is negligible, this leads to

$$Jny = q\,\mu n\, n\, Ey = -q\,\mu n\, n\, dV/dy \qquad \text{Eq 2.1.10}$$

where n is the inversion carrier density, V is the channel voltage, q is the charge of an electron, =1.6e-19 coulomb and μn is the mobility. The current is therefore

$$Ids = -\iint Jny\, dx\, dz = -W \int Jny\, dx$$

$$Ids = (-W\, dV/dy)\,(-q \int \mu n(x,y)\, n(x,y)\, dx) \text{ from } 0 \text{ to } Xc \qquad \text{Eq 2.1.11}$$

Xc is the channel depth.

$$Qn(y) = q\ N(y)$$

N(y) is the inversion carriers and $=\int n(x,y)\, dx$ from 0 to Xc. This leads to

$$Ids = -W\,\mu n\, Qn\, dV/dy$$

Solving the differential equation

$$\int Ids\, dy = Ids\, L = -W\,\mu n \int Qn\, dV \text{ from } 0 \text{ to } V \qquad \text{Eq 2.1.12}$$

Qn can be found to be -Cox(Vgs - Vt). Across the channel, the effective voltage is position dependent in the Y direction and equals 2Φf + V where 0<V<Vds. This means that Vgs must be V higher to achieve the same level of Qn. Therefore Vg should be replace with (Vgs - V), leading to

$$Qn(y) = -Cox\,(Vgs - Vt - V)$$

$$Id = -(W/L)\,\mu n \int -Cox(Vgs - Vt - V)\, dV \text{ from } 0\ Vds$$

$$Id = (W/L)\,\mu n\, Cox\,[(Vgs - Vt)\, Vds - (Vds\text{^}2)/2] \qquad \text{Eq 2.1.13}$$

In the saturation region, the Vds dependence is negligible. This leads to

$$Id = Idsat = (W/L)\,\mu n\, Cox\,(1/2)\,(Vgs - Vt)\text{^}2 \qquad \text{Eq 2.1.14}$$

With this understanding of the expected MOS transistor curves, comparisons can be easily made and differences can be referenced to variances in the theory for high power devices.

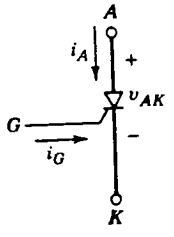
2.2 High Power Devices

2.2.1 BJTs and Thyristors

The history of high powered semiconductor technology can be seen to actually predate that of computer integrated circuits. With the invention of the power device, over 35 years ago, there has been a strong driving force to increase their voltage and current handling capabilities. Today's power thyristor is capable of handling up to 6500 Volts and 2000 Amps.

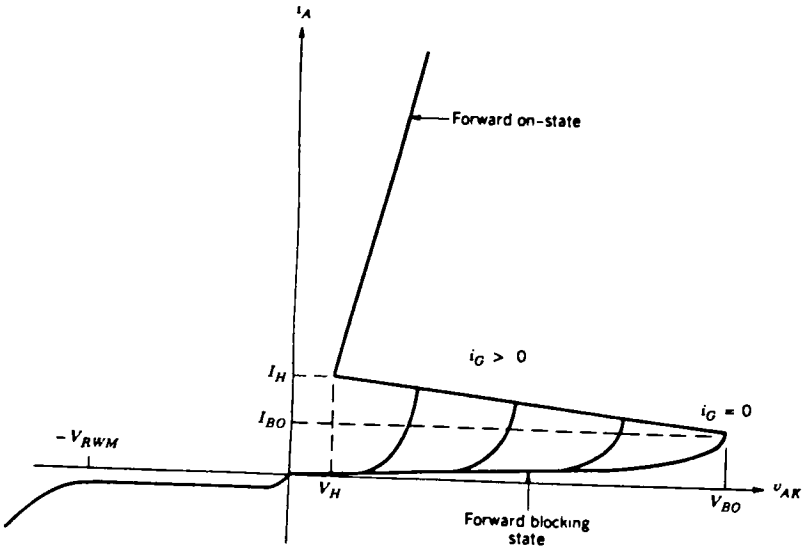
The primary operation of the high powered device is to act as a switch. Although the BJT and GTO thyristor differ from standard thyristors due to there operational controllability and fall into the same category as the power MOSFET and IGBT, they are considered with the thyristor due to their limited applications in PICs. Thyristors are latched on by control signals but must be turned off by the power circuit.(1) The reason for this will become apparent shortly. The BJT and GTO thyristor are turned on and off by control signals.(1)

The circuit symbol for the thyristor and its I-V characteristic curve are shown in Fig. 2.4 and Fig. 2.5.



Circuit symbol for the thyristor

Fig. 2.4

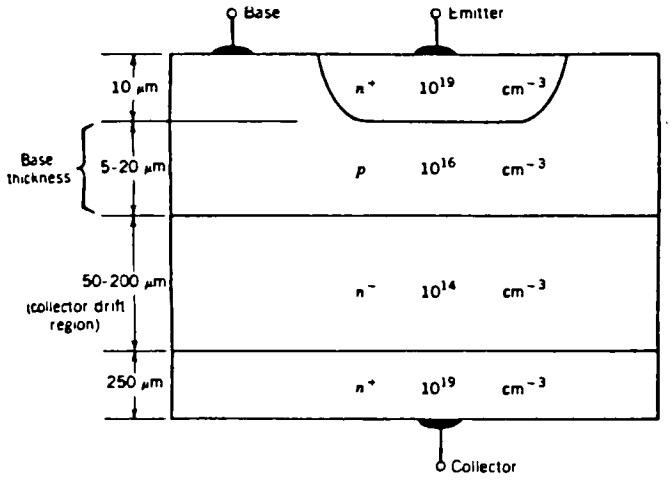


Plot of current vs. applied voltage showing negative resistance region and effects of gate current

Fig 2.5

The thyristor is a four or five layer silicon device depending on the desired current flow capabilities. For this discussion, a single direction current flow device is used. The thyristor can be triggered into the on state by applying a pulsed signal to the control gate, provided the device is correctly biased. Once in the on state, the gate current can be removed without turning off the device. The device can only be turned off by reducing the anode current to zero or to a negative value. There are many types of thyristors but all fall into this basic operation type.

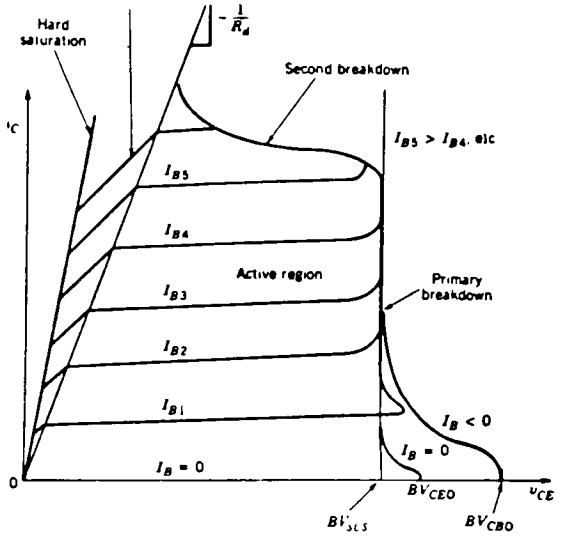
The power BJT has a different structure than its low power logic level counter part. Fig 2.6 is provided to illustrate these differences and to show an important problem with both the power BJT and the thyristor for applications in PICs.



Cross section of the vertical Power BJT

Fig. 2.6

First, the power BJT needs to incorporate a drift region to accommodate the large voltages and currents. This results in a slightly different I-V characteristic which is shown in Fig. 2.7.



Ic vs. Vce family of curves for the Power BJT showing more resistive region

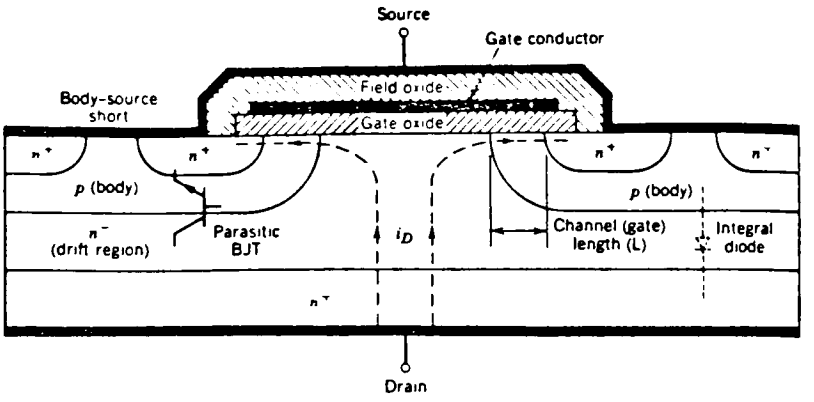
Fig. 2.7

At this point it should be noted that the gain of a power device in general is quite less than its low power counter part. This is due in part to the drift region resistance which required the control circuit to provide large amounts of current by control standards to drive the power device.

The other important thing to note from Fig. 2.5 is that the junction depths range from 10 to over 100 microns. This is incompatible with the junction depths of the low power control circuitry. For these two reasons PICs look to power MOSFETs and IGBTs.

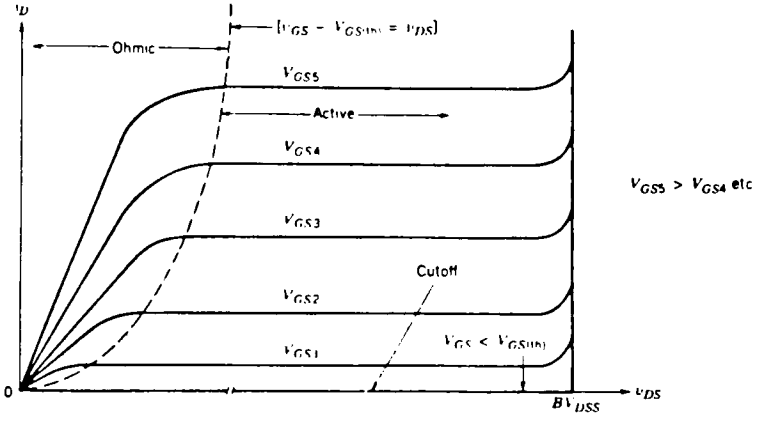
2.2.2 Power MOSFETs and IGBTs

With the development of the power MOSFET in the early 1980's, the incorporation of power devices and control circuitry has been greatly increased. This is the bases for the objectives of this thesis. The power MOSFET feature a high input impedance, high switching speeds, ease of paralleling to produce greater current flow, a greatly increased Safe Operating Region over other power devices and control level drive capabilities. The power MOSFET is not capable of the high end power handling that the previous devices were but does provide mid and low range power handling. The cross section of a power MOSFET is presented in Fig. 2.8 and the I-V characteristics are shown in Fig. 2.9.



Cross section of the vertical Power MOSFET

Fig. 2.8



Ids vs. Vds Family of curves for the Power MOSFET

Fig. 2.9

Again the lightly doped drift region should be noted. This region acts similarly to that found in a PiN diode. During the blocking mode, the depletion region length can be determined by Eq 2.2.1. See Fig 2.9 for depletion region locations.

$$Xd = Xp + Xi + Xn$$

$$= [(2\mathcal{E}s/q)(1/Na + 1/Nd + 1/Ni)(\Phi i + Va)]^{1/2} \qquad \text{Eq 2.2.1}$$

The doping levels of the regions now become important. Assuming that the drain is doped higher than the channel and that the channel is doped higher

than the drift region as would be the case in both the PiN diode and the power MOSFET, Eq 2.2.1 can be simplified to Eq. 2.2.2

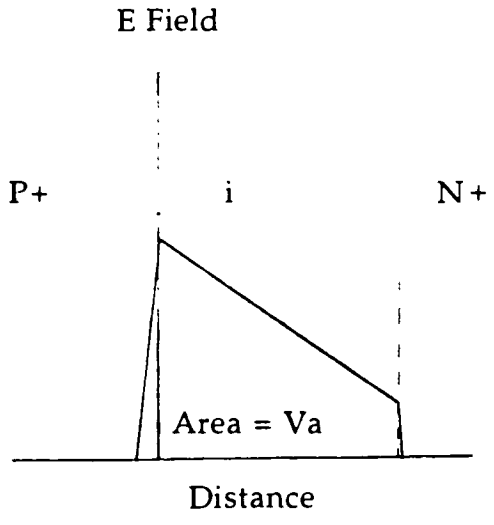
$$Xd = Xi$$

$$= [(2\mathcal{E}s/qNi)(\Phi i + Va)]^{1/2} \qquad \text{Eq 2.2.2}$$

It can be seen that with out the Ni doping the depletion length would be considerably smaller. Also Eq 2.2.2 assumes that the applied voltage, Va, is not substantially large to force the depletion region in the channel to approach the drift region length. The size of the depletion length is of importance due to the relationship between the electric field, the applied voltage and the depletion length, see Eq. 2.2.3

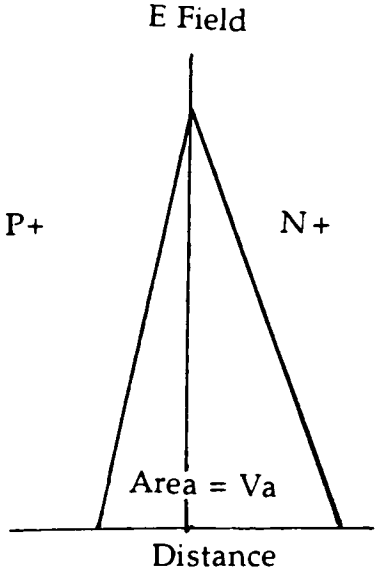
$$Emax = 2(\Phi i + Va)/Xd \qquad \text{Eq 2.2.3}$$

As the depletion length decreases, the electric field increases. As Emax reaches Ecrit the junction of the device will breakdown. A graphical depiction of the PN junction with and without the drift region is shown in Fig. 2.10 and Fig 2.11.



Electric Field vs Distance for a PiN Structure

Fig 2.10

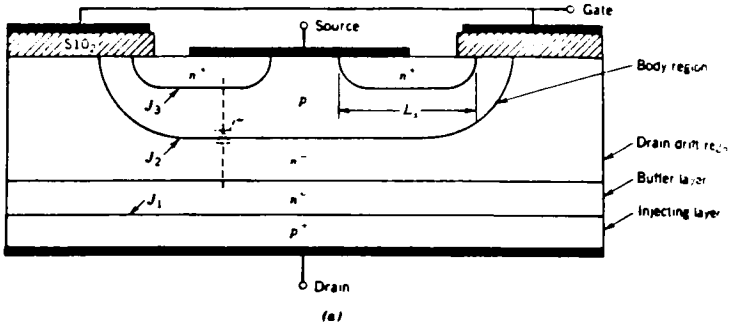


Electirc Field vs distance for a PN Structure

Fig 2.11

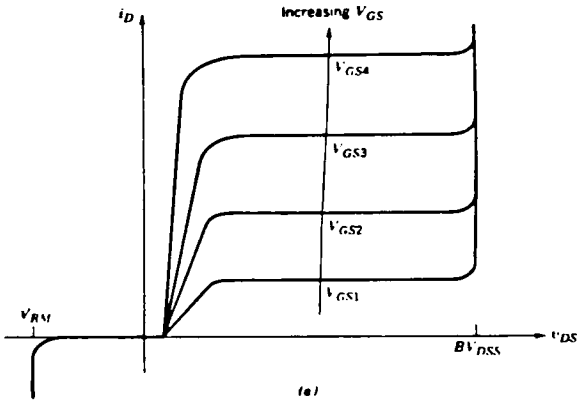
Although the cross section of Fig. 2.7 shows a vertical power MOSFET, lateral devices are possible and operate on the some principles but at a reduced voltage and current handling capability. For the design and fabrication of power devices in this thesis a lateral design was chosen for reasons that should become apparent later.

One problem with the power MOSFET, as mentioned before, is its inability to provide large amounts of current without the use of large die areas. This has been remedied by the development of an Insulated Gate Bipolar Transistor or IGBT. This device seeks to incorporate the best qualities of both the MOSFET and the BJT. The cross section of this device is similar to that of the power MOSFET, with the exception of an added P+ to the drain, for NMOS devices. Note that in the figure below, the P well which forms the channel is shorted to the source. The cross section is shown in Fig. 2.12 and the I-V characteristic is presented in Fig 2.13.



Cross section of lateral IGBT Device

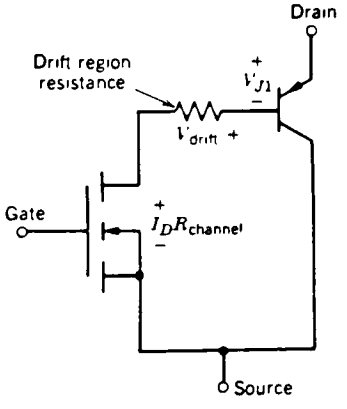
Fig 2.12



Id vs. Vds family of curves for the IGBT

Fig. 2.13

The P+ layer at the drain causes several things to occur. First, the resistance in the linear region of the I-V curve is reduced. When the PN junction at the drain region is forward biased, minority carriers are injected into the drift region. A larger current is produce from the drain to the source because of the increased conductivity and the lowered on resistance. An equivalent circuit for the IGBT is shown in Fig 2.14.



Circuit equivalent for the IGBT device

Fig. 2.14

The improvement in the on resistance depends on the doping of the drift and P+ regions as is the case in the BJT. Where the power MOSFET is subject to parasitic BJT turn on or latch up, the IGBT is subject to a parasitic thyristor turn on or latch up. The IGBT is also subject to premature turn on without

gate stimulation if the operating voltage is applied to quickly. This limits the frequency of operation for the IGBT. Although the IGBT shows an improvement over thyristors in operating frequency the MOSFET is superior in this aspect.

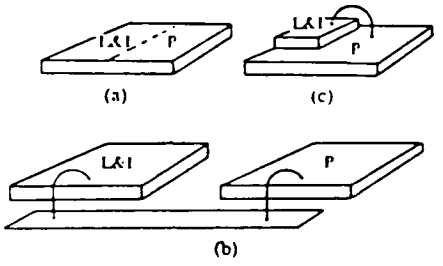
These devices do not require large junction depths and are possible to fabricate with the same procedures as those of low powered devices. For this reason they are well suited for applications in PICs.

2.3 Mixed Power Circuits and Devices

There are several ways in which the low and high powered devices can be coupled together. These are important to understand because they do place some restriction on the PIC being designed.

The first type of isolation is a chip on chip or multichip module approach. These are actually slightly different in packaging but are similar in concept. In the chip on chip technique, the power device and control circuits are produced on separate silicon wafers. These wafers are then sectioned into devices. An oxide layer is grown on both devices and they are directly bonded to each other by the oxide. [4] This oxide is used to isolate the power and control devices. Due to the nature of the oxide, any power end voltages and currents that would be harmful to the control circuitry is prevented from reaching the control circuitry. This type of isolation is known as dielectric isolation.

Multichip modules again start with the power and control circuits being produces on separate wafers. The devices are then sectioned and mounted on a ceramic substrate instead of on each other. [6] As can be seen, the devices are not in contact so that there is no possible parasitic interactions between devices, with exclusion of the interconnects. Fig 2.15 shows they multichip module approach in (b) and the chip on chip approach in (c), (a) depicts the following three forms of isolation.



PIC assembly configurations: (a) Monolithic; (b) Hybrid; (c) Chip-on-chip

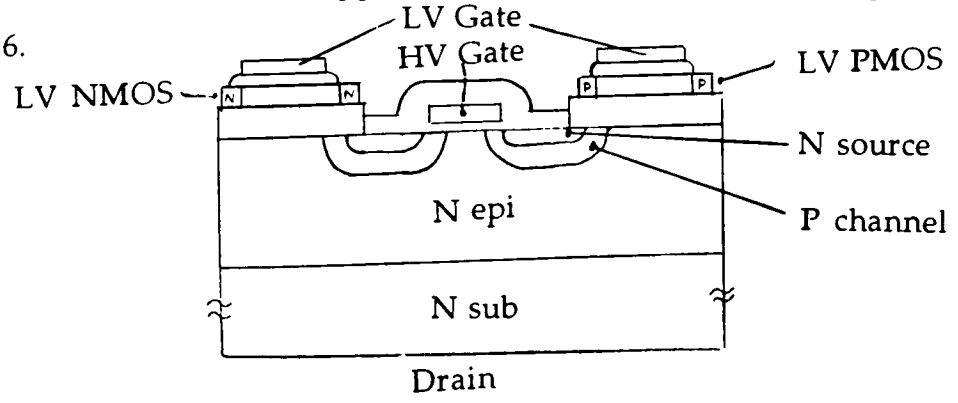
Fig. 2.15

These approaches provide excellent isolation but there are several concerns as to cost, size, interconnects and mounting. Due to the nature of fabrication using two processes, the cost per device is increased. This is inherent in silicon fabrication due to yield losses and processing materials. The size of the device is larger than that of the other isolation methods. Also, with the need of very fast feedback for protection reasons, the types of interconnects must be able to accommodate this. The interconnects are noted for parasitic inductances which limit the driving frequencies. The parasitic inductance causes large power spikes during switching. With the reduction in the inductance the power spikes are also reduced. The use of these interconnects also requires an increase in processing. The bonding to the ceramic must be able to handle this heat and not result in bond breaking. The

chip on chip method must be able to deal with the thermal stress that is produced and not result in wafer breakage.

Finally, it should be noted that these methods place no restrictions on the types of power and control circuitry that could be used. This is very important for increasing the application range of Intelligent Power Technology.

The second method that is in use for isolating the control electronics from the parasitic effects of the power devices is to build thin film polycrystalline silicon transistors on the field oxide of the vertical power devices. This technology allows for MOS transistors as well as polysilicon diodes and resistors. The formation of the control circuitry can be accomplished with no change to the thermal budget of the power device thus the characteristics of the vertical device are not compromised. [5] The heat produce from the operation of the power device has little effect on the operation of the low power transistors due to the field oxide. This means that there is no increase in processing complexity or reduced performance of the power device with this approach. A cross-sectional view is presented in Fig 2.16.



Cross section of thin film transistors on field oxide isolation method

Fig 2.16

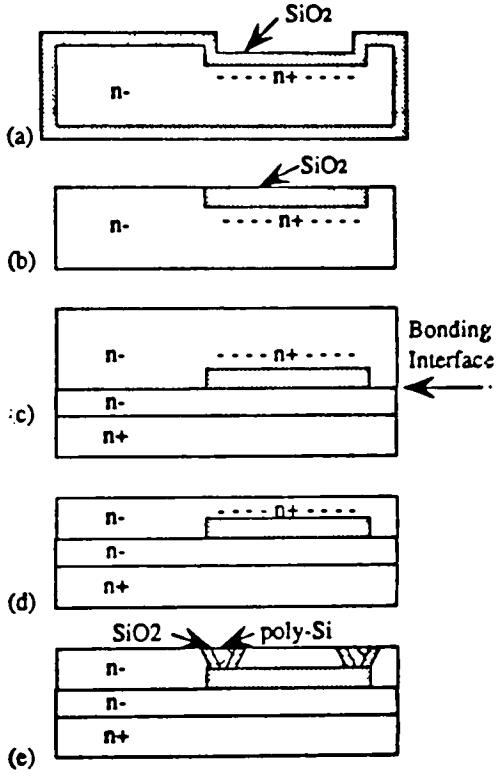
This method has several advantages over other methods. As was already mentioned, there is no increase to processing complexity and a minimal increase to the number of processing steps. This results in a reduced cost compared to other methods and an increase in production time. Also, the use of the field oxide to provide insulation is quite successful for this purpose. On the other hand, this approach does have several drawbacks that must be considered by the designer.

First, the use of polycrystalline silicon for the thin film transistors is not without its problems. The polycrystalline silicon transistors are of poorer quality than those produced of standard silicon. This is due to an increase in trapping states at the grain boundaries. [5] This poorer quality could result in devices that are less than optimal. This is a serious problem if precision control is needed. Also there is more of a temperature dependence in this isolation method. This means that the application range is reduced to lower temperature applications or temperature limiting circuitry is needed. The final concern for the designer is the range of control circuitry that is available. Since bipolar devices can not be produced, the designer must follow a strict CMOS design.

The third type of isolation is a combination of both the wafer bonding, chip on chip and the oxide isolation just discussed. The processing steps are displayed in Fig. 2.17

Initially a trench is etched into a silicon wafer. The area of the trench is implanted to produce an N+ layer. Next an oxide is grown, refer to Fig. 2.17.a. The wafer is then polished, inverted and mounted to another

wafer. This is depicted in Fig 2.17.b and Fig 2.17.c. It should be noted that the bonding process is done without the growth of oxide between the wafers. This is crucial for the operation of the power device. This type of mounting allows for the power device to be built through the entire wafer package and could result in simpler processing. The lack of oxide at the wafer interface is what differs this from the chip on chip method. The wafer is again polished and a guard ring trench is then etch. This trench surrounds the original trench and is shown in Fig 2.17.d and Fig 2.17.e. The guard ring trench is filled with silicon oxide and poly. [6] This completes the isolation process.



Fabrication method for wafer bonding isolation method

Fig 2.17

It can be seen that this process has many advantages. First, the control electronics can now be built on crystalline silicon thus improving its performance capabilities over those of the thin film transistor previously

mentioned. Also the power device is able to be both lateral and vertical in nature. The control area of the chip can support both MOS and bipolar electronic components, allowing for more design freedom. Finally, the low parasitic capacitance, high voltage isolation and resistance to latch up are excellent.

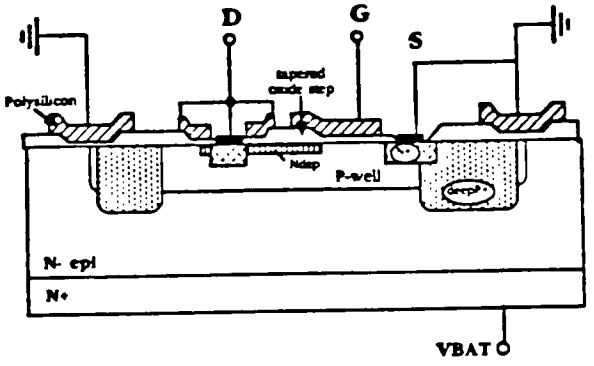
The only disadvantage to this type of isolation is its complexity and the associated higher manufacturing cost. As can be seen from the process description, there are several polishing and lithography steps added, which result in longer processing times. The added cost is not only for increased processing but for the higher quality wafers that are needed due to the polishing steps. [7]

The final isolation method to be discussed in this report is a form of junction isolation based on a Floating Well design. This form of isolation is based on reverse biased junctions, whereas the preceding forms have been based on dielectric isolation. In junction isolation, a heavily doped region is placed around the critical areas of the devices. This helps in several ways and can be seen to incorporate itself with the power device fabrication methods easily. As the power device already requires the formation of P+ doped regions. Junction isolation can utilize this P+ implant and thus require no increase of process complexity or processing steps. A related advantage of this process simplicity is that it can be easily duplicated at most experienced production facilities.

However, there are several concerns also associated with this method. First, due to the nature of the isolation, which will be discussed shortly, this

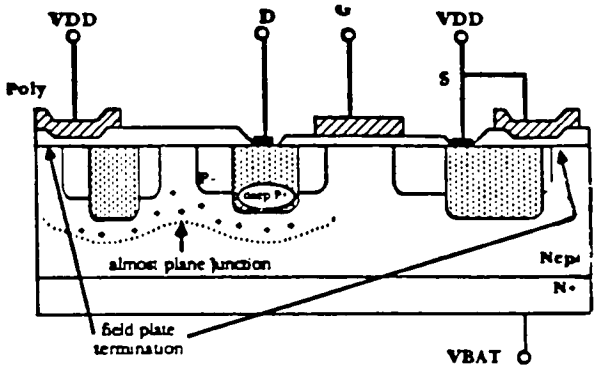
method is not suited for very high power isolation. Also, the designer must keep in mind that this technique is more susceptible to latch-up.

The floating well isolation handles the latch up concern in two ways. First, by allowing the well to float, it could follow any voltage transient that occurs, thus avoiding the turn on of the Parasitic Vertical Bipolar Transistor or PVB. Secondly, if the PVB is activated, the base current is only provided during a limited time which is less than the latch up regeneration time. [10] The performance of the floating well isolation method is enhanced by the addition of the deep P+ plug. Refer to the Fig 2.18 and Fig 2.19 Note that Fig 2.18 is for high powered devices and Fig 2.19 is for low powered devices.



Cross section of the silicon implementation of a high voltage NMOS transistor with its static and dynamic shielding

Fig 2.18



Cross section of the silicon implementation of a low voltage PMOS transistor with its static shielding

Fig 2.19

The P+ well serves several function. First, it reduces the gain of the Source PVB. This is done by the N+/P+ emitter - base junction, which causes a large amount of recombination, thus reducing gain. The heavily doped base provides a large quantity of recombination centers which work to trap electrons and reduce the current flow through the device. This reduced gain prevents the turn on of the PVB and stops latch from occurring. In order to prevent the turn on of the Drain PVB the P+ well is used in a thin capacitor set up similar to a RC circuit. The capacitor set up can be designed so that any voltage disturbance coupled to the P- well is attenuated to values low enough to prevent triggering of the PVB. [11] This attenuation is accomplished with the RC circuit acting like a filter. Finally, the P+ well helps to increase the breakdown voltages of all devices. By spreading the source P+ well around the drain, a more planar junction is produced. This planar junction is less

susceptible to breakdown due to the lack of sharp corners which reduce breakdown.

This type of isolation also incorporates a field plate to increase the junction breakdown. A field plate is a conductive layer that is attached to the gate of the device and overlaps the junction over an oxide film. In a P source/ Nwell configuration, it can be seen that without the field plate the depletion region, which is desired to be large to stop breakdown, is narrower at the surface of the chip. This narrowing is due to the positive oxide charge that attracts the electrons in the Nwell. By using a field plate, a MOS capacitor is formed over the junction. This capacitor acts to deplete the surface thus increase the width of the depletion layer in this region, see Fig 3.5 on page 29. A risk of using the field plate is breakdown of the gate oxide due to large potential differences from gate to drain. The field plate must be optimized for best performance.

Junction isolation holds many advantages that can be utilized to their fullest extent if proper planning and design techniques are used. The concerns for latch up can be addresses. Due to its reduced cost and good performance capabilities, this isolation method will continue to see increased use especially in moderate power device application in large volume consumer products. This form of isolation is to be used in this thesis due to its practicality and quality.

Junction isolation allows for some protection of the device to be provided by the circuitry on the chip. Several of these circuits are commonly found in most mixed power designs. These will be mentioned and described

briefly. It should be apparent that these circuits are already found in strictly low power designs. The incorporation of the protection circuitry is not complicated because new circuits do not need to be designed.

When interfacing high and low powered devices it is important to drive the high power device into saturation. This is often achieved with a charge pump. This circuit allows for a greater voltage to be applied than that of the supply rails. It is utilized commonly in EEPROM devices for programming and erasing purposes. Another common device for interfacing is the level shifter. This allows output signals from the low power circuitry to be adjusted for direct application to the high power device.

In order to protect the low power devices from the transients of the high powered device low power MOSFETs could be used in a configuration where the gate is shorted to drain. As the current increases rapidly due to transients impact ionization would occur and act to reduce the current. This is only conceptual and the process is more complicated than described here. Another form of device protection is with the use of Zener diodes. As the voltage increases to a destructive level, the Zener diode would breakdown thus protecting the device. Both of these methods are used with some regularity.

There are many in line protection circuits that can be incorporated. Circuits to reduce electromagnetic interference throw drive signal shaping; temperature sensing using diode turn on; Hall effect sensing; and current sensing amplifies are some of the most common forms of protection. All of which can be found in low power circuitry already. It is not in the scope of

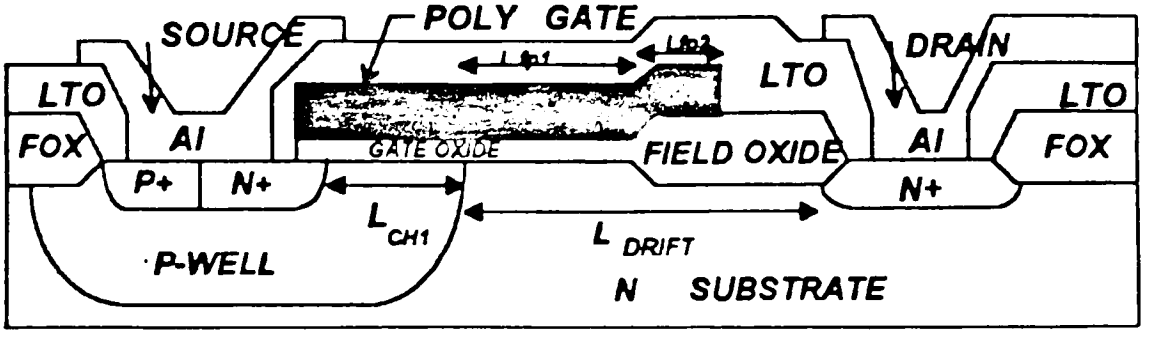
this thesis to study these, therefore they are only mentioned as examples and it is up to the reader to investigate them further.

The scope of this thesis is to develop a power device that maybe used in PIC components. The initial work is based on a lateral power device design and investigates methods to increase the breakdown voltage and reduce the on resistance of these devices. The following sections present the theory and simulation used to design the power device. Also presented is the design layout technique and fabrication procedure. Electrical analysis and future work conclude the report.

3. Theory and Simulation

3.1 Theoretical Characteristics

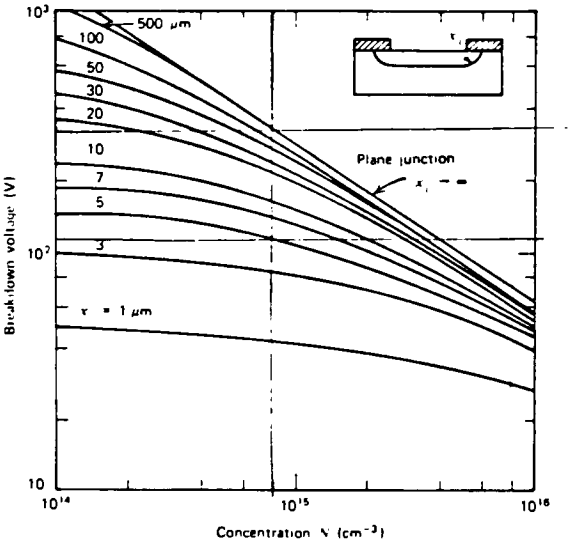
A cross section of the Power MOS to be designed is in Fig 3.1. The calculation for the drift region, the field plate overlap and the well curvature are based on this cross section.



Cross section of the vertical Power MOSFET

Fig 3.1

The standard RIT CMOS process was used as a base line for the power device. This process uses a 5 - 15 Ω-cm N type wafer as the substrate. The 5 - 15 Ω-cm translates into a doping of Nd = 8e14 cm-3. From Fig. 3.2 the breakdown voltage may be determined.



Breakdown voltage of one sided, plane, silicon step junction showing the effects of junction curvature

Fig. 3.2

Reading from the figure, for a junction depth, Xj, the maximum breakdown voltage that could be expected is Vbreak = 325V. The RIT CMOS well junction depth is reported to be approximately Xj-well = 5μm and the resulting breakdown would be Vbreak = 110V. At this point the decision to use a field plate was made. With the use of a field plate, the effective curvature of the depletion layer could be expected to be increased beyond 5μm resulting in a Vbreak in excess of 110v. With an effective depletion layer curvature of 6μm to 7μm, a breakdown voltage of 150V to 200V could be expected. Allowing for modeling errors or surface non-idealities, breakdown voltages exceeding 100V should be achieved.

Allowing for a possible breakdown voltage, Vbreak = 150v, a depletion width of

$$Xd = (2\,\varepsilon si\,Vbreak / q\,Nd)^{1/2} \qquad \text{Eq 3.1.1}$$

$$= 15.3\mu m$$

is needed. Similarly a 100V breakdown would require approximately 12.5 μm of depletion width. The depletion layer should be accommodated within the drift region. If the drift region is not long enough, the occurrence of the reach through condition would start to degrade the voltage blocking capability of the device. However, too long of a drift region would cause excessive on state resistance. Allowing for limited reach through gives a good compromise between BV and Ron. For this initial trial the drift region length was fixed at 10μ.

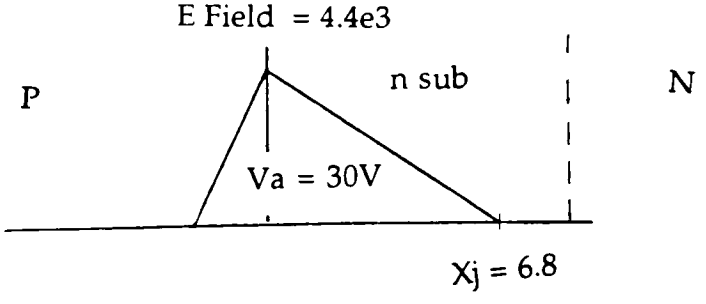
Next, the gate oxide thickness was chosen to be 1000Å. The critical electric field value for RIT's oxide is reported to be 3 MV/cm. This leads to a calculation for the maximum voltage allowable across the thin gate oxide after which breakdown will occur.

$$E_{critical} * t_{ox} = 3\ MV/cm * 1e\text{-}4\ cm = 30\ v \qquad \text{Eq 3.1.2}$$

This leads the application of Eq 3.1.1 with the critical voltage to find the maximum extent of the field plate.

$$X_{j\text{-}field} \leq 6.8\mu$$

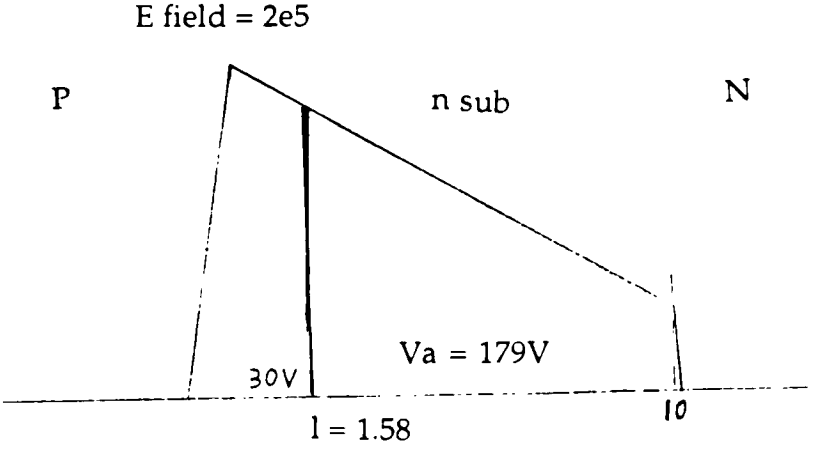
Allowing for errors, the field plate extension is limited to under 5μ. Fig 3.3 shows the Xj-field for 30V from drain to source.



Plot of Electric Field vs. Distance around PN junction when 30V is applied

Fig 3.3

Xj-field is the depletion region distance. Although this length was used in the trial run, it is not the correct distance for the field plat overlap. The depletion region distance for 30V and the 30V distance when 150V are applied are not the same. To determine the 30V distance when 150V are applied refer to Fig 3.4.



Plot of Electric Field vs. Distance around the PN junction showing the extent of 30V into the drain

Fig 3.4

Assume a maximum electric field of 200,000 V/cm. The total area under the curve in Fig 3.4 is equal to 150V. The portion of the curve with an area of 30V will determine the length of the field plate overlap and is the distance, l, in Fig 3.4. As previously stated, the slope of the line is q*Nd/εs. The electric field at a distance, l, is:

$$q^* Nd / \varepsilon s = 1.25e8 \text{ V/cm}^2$$

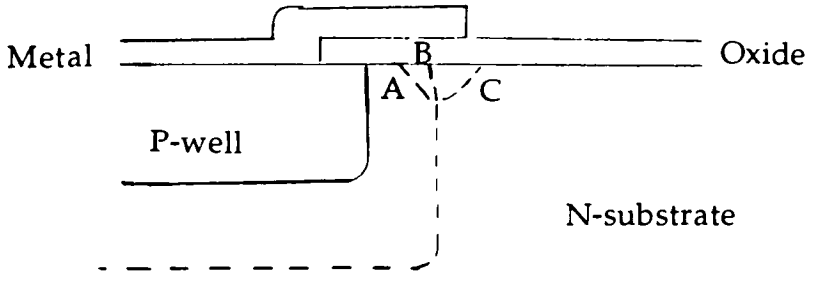
$$E(@l) = (2e5 - 1.25e8 * l)$$

An average value of the electric field was determine. This value multiplied by the distance, l, was equated to 30V. l was solved for by the quadratic equation and the maximum overlap was determined.

$$30 = .5(Ecrit + E(@l)) * l$$

$$l = 1.58\mu m$$

With the well designed for breakdown and an idea of the length for the field plate a better explanation of the operation of the field plate is presented. The electric field at the surface of a planar diffused junction is higher because of depletion layer curvature effects. The depletion layer curvature can be controlled by altering the surface potential. By altering the potential on the field plate, the depletion layer shape can be adjusted by the MOS capacitor effects. The oxide layer over the channel has a positive charge which acts to attract electons to the surface decreasing the depletion region at the surfaceshown in case B. Referring to Fig 3.5, when a positive bias is applied to the gate field plate with respect to the N substrate, it will attract electrons to the surface and cause the depletion layer to shrink as illustrated by case A. If a nagitive bias is applied to the field plate, it will drive away the holes from the surface, causing the depletion layer to expand as shown in case C. The curve in C can be seen to have an increased depletion width. This makes the electric field spread over a longer distance. For a given voltage the, the increased spread lowers the local electric field value. This acts to postpone avalanche multiplication of the carriers and breakdown. As the voltage is increased on the field plate, the breakdown voltage of the planar junction can be made to approach the parallel plane value. (24)



Cross section of PN junction showing the effects of a field plate overlap

Fig 3.5

As the oxide thickness increases, the influence of the field plate on the depletion region curvature becomes smaller. This fact is used to move the high electric field point from the NP junction yet not produce a significantly high field across the gate oxide at the end of the field plate and not produce a high field point at the end of the extended depletion region due to the curvature at that point.

Another consideration for the field plate is the extent of the overlap. With the drift region distance fixed, the increase of the field plate causes a reduction in the field oxide length. The length of the field oxide is the distance over which the high voltage is reduce before exposure to the thin gate oxide. With the reduction of the field oxide length, the distance in which the voltage is reduced is decreased. This decreased distance results in larger electric fields. The length of the field oxide is limited by the electric field and the breakdown of the device. This is studied in both the simulation and the fabricated devices.

In order to determine the width of the device needed for approximately 0.5 A of current, Eq 2.1.14 was applied with values typical for the R.I.T. facility. Typically, μn = 40 $\mu m^2/V\text{-}s$ and Cox = 0.345 $fF/\mu m^2$. Therefore, for a Vt = 2v and a channel length, L, = 5μm:

$$Id = Idsat = (W/L)\,\mu n\, Cox\, (1/2)\,(Vgs - Vt)^2 \qquad \text{Eq 2.1.14}$$

$$0.5e6 = [W*40*0.345*0.5*(6-2)^2] / 5$$

$W \approx 4500\ \mu m$ for a drain current of 100mA.

For 500 mA the required channel width would be:

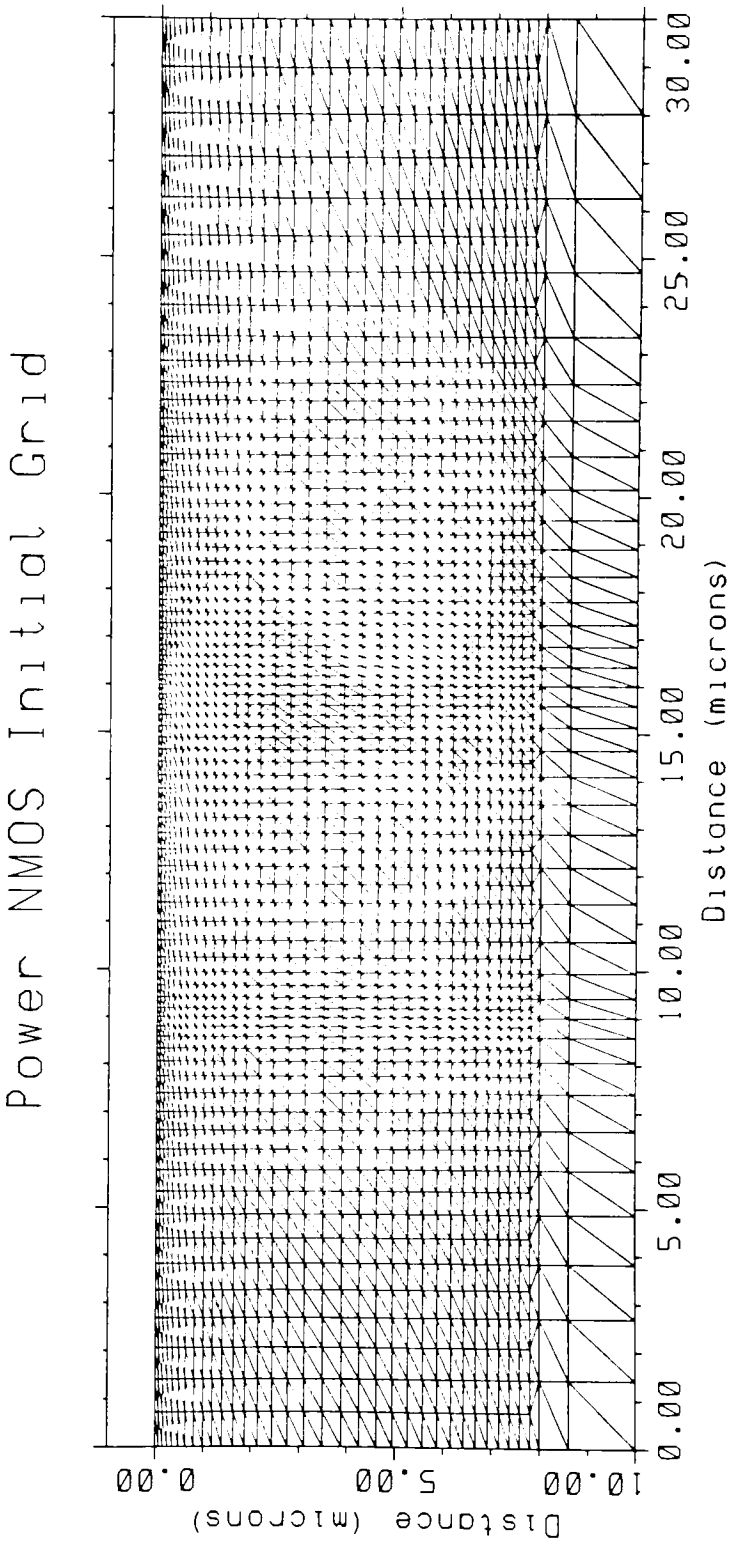
$W \approx 22500\ \mu m$

3.2 SUPREM 4 and MEDICI Simulation

Lateral power devices rely on the extent of the lateral diffusion to define the length of the channel region. For this reason two dimensional process and device simulations are necessary. SUPREM 4 and MEDICI, both from TMA, were used for simulations.

The actual SUPREM 4 input and output files are found in Appendix A. Appendix A also contains a table of simulated junction depths and other measurements of interest. The primary objective of this simulation was to investigate the shape and size of the P-Well which forms the channel. As stated before, the shape or curvature of the well would directly affect the breakdown voltage. The amount of lateral diffusion was needed for the chip design. The drift region was set to a fixed distance and the amount of lateral diffusion directly affect where the drift region should start.

There are several concerns that needed to be addressed with the use of SUPREM 4. First, the output was to be imported by MEDICI for electrical analysis. The MEDICI structure file or input from SUPREM 4 is limited to 3200 nodes. Therefore, when specifying the node mesh in SUPREM 4, care must be taken to meet this requirement. Fig 3.6 shows the initial mesh for the power devices under study.



Power NMOSFET initial grid

Fig 3.6

Next, for the most part, the ramp up and down portions of the diffusion steps have little effect, therefore most were not included in the simulations to decrease the simulation time. On crucial steps, such as the Gate Oxide growth, the ramp rates were included from the actual run data and the simulations were rerun for a more accurate analysis.

The last major concern is in the etch steps. These steps do not account for lateral etching and therefore may cause some deviations form actual device sizes. This must be designed for.

With the device structure generated by SUPREM 4, the electrical analysis may be performed with the MEDICI software. The actual input and output files are included in Appendix B. The primary objective of these

simulation were to study the points of high electric field to determine breakdown and to determine expected current and voltage capabilities. As with SUPREM 4, there were several concerns that needed to be taken care of before the MEDICI software was able to operate correctly.

First, due to the high power nature of the devices being simulated, the software encountered numerous convergence errors. This meant that the solutions obtained for one node point did not coincide in the allotted number of iterations. Several things were done to solve this. First, the number of iterations were increased. Second, if a solution was not initially obtained based on the first approach, the software looked at half of the original value being solved for. A solution at the half value was found so that a better approach could be made for the original point. This half value was reduced

to 0.2 of the original value to improve the convergence of the numerical algorithms. Finally, the tolerances of the convergence criteria were widened.

The simulation of the IGBT posed another problem. The MEDICI software was unable to converge no matter what was done. It is surmised that the nature of the IGBT is either too complex or, more likely, the software does not have the capability to handle four layer devices with the negative resistance regions that are present in their I-V characteristics.

The lateral Power MOSFET was simulated under fifty volts from drain to source and five volts on the gate. The initial results showed that the device did not turn on. The simulation was rerun and a plot of the potential, the electrons, the holes and the electric field were plotted. This revealed that the threshold adjust implants were isolating the drain and forming a five layer device. The SUPREM 4 simulation was then altered so that the N+ source/drain implants were implanted deeper into the device. The cause of the isolation was the added thermal diffusion from the increased gate oxide thickness.

The device was again simulated under a Vds of 50V and Vgs of 5V, the well and source were tied together. The result from this simulation are shown in Fig 3.7 through Fig. 3.12. For these plots, it should be noted that the darker the color, the larger the value at that point for the quantity of interest. For example, on the electron volume density plot the darkest areas are in the source, drain and channel as would be expected. The threshold voltage was obtained from the Ids vs. Vgs plot shown if Fig 3.13. A threshold voltage of 1.75V was taken from the plot. A simulation of the expected I-V characteristic

was also generated in Fig. 3.14. An on resistance of 5.6Ω was fround from this plot.

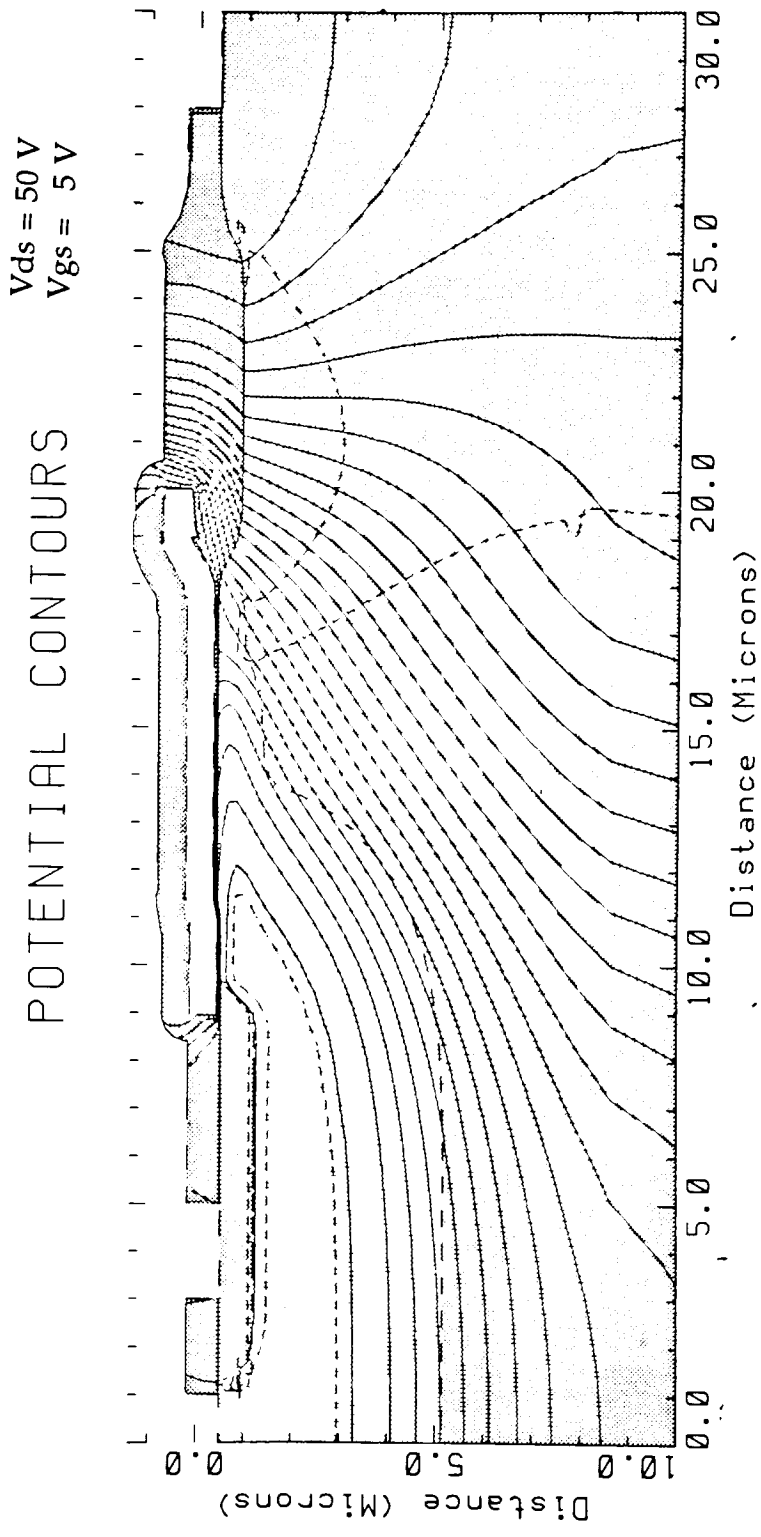
Regarding the off-state of the device, the simulations were repeated for a Vds of 300V and a Vgs of 0V. The plots of the potential lines, the current, the electrons, the holes and the electric field are shown in Fig 3.15 to 3.19 respectively. The electric field plot was used in determining the location of the highest electric field point in the device.

The device was re-simulated in SUPREM 4 to produce the longer field plate extension. Again the MEDICI program was run and the effect on the electric field were investigated. In Fig 3.20 and Fig 3.21, it is shown that the longer field plate does produce higher electric fields. The areas were this happens are enlarged in the plots. The darker the region, the higher the concentration of the electric field. Fig 3.20 is for the shorter field plate.

Again the SUPREM 4 was used but the drift region was increased on order to achieve a higher breakdown voltage. The MEDICI plots are shown in Fig 3.21 to Fig 3.28. The output I-V curve is in Fig 3.29. The threshold adjust implant was removed for this simulation so that future work could use it as a reference. The resulting on resistance for this device was 7.2Ω or an increase of 26.3% over the shorter drift region.

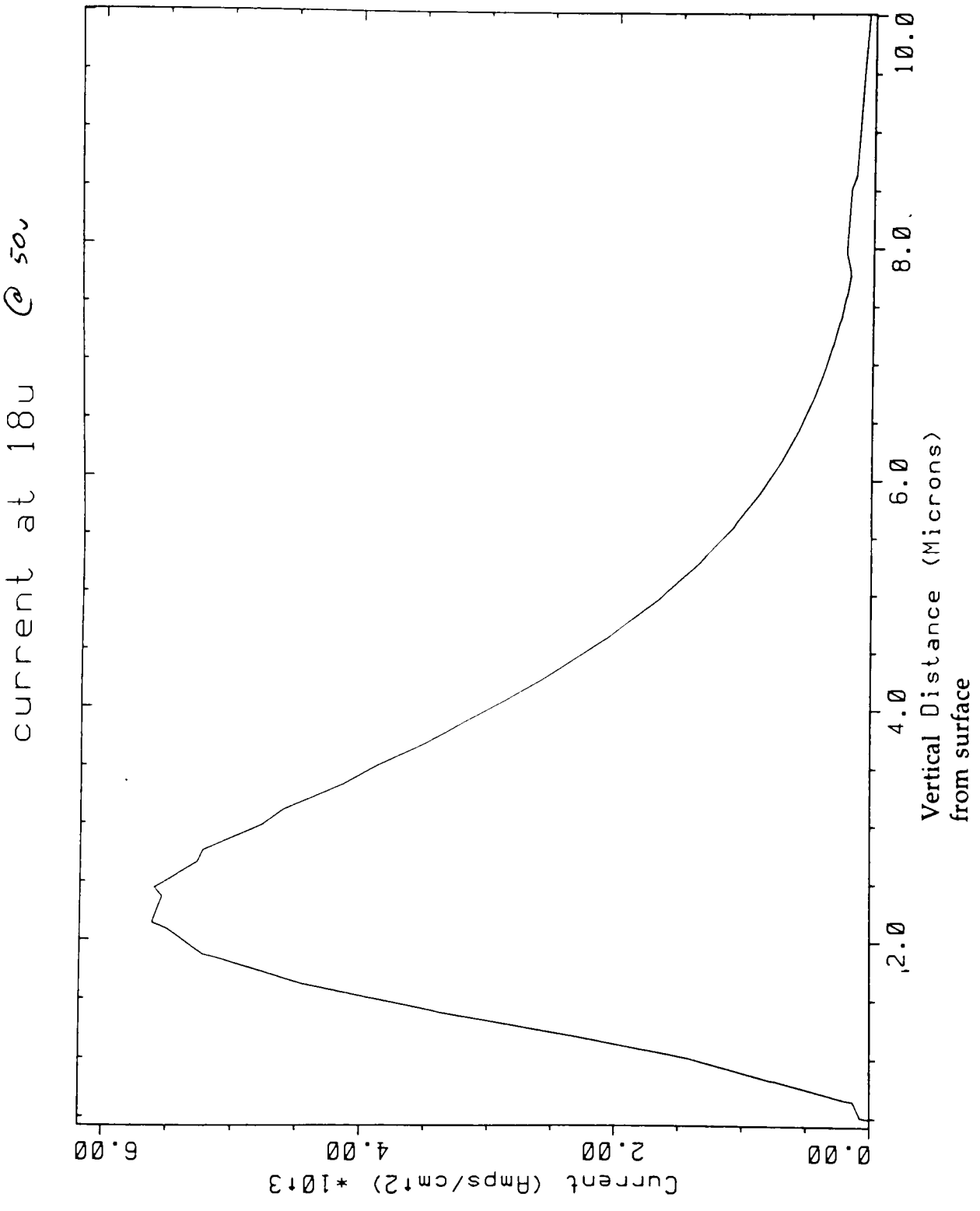
The breakdown voltage of the device was simulated by increasing the drain to source voltage to 400 Volts with no voltage on the gate. The breakdown was found to be approximately 350 Volts. This is the ideal breakdown for a planar junction at 8e14 doping. This is shown in Fig 3.30.

Simulations that were done to determine the effects of the P+ and N+ implants overlapping indicated no significant differences in any of the plots.



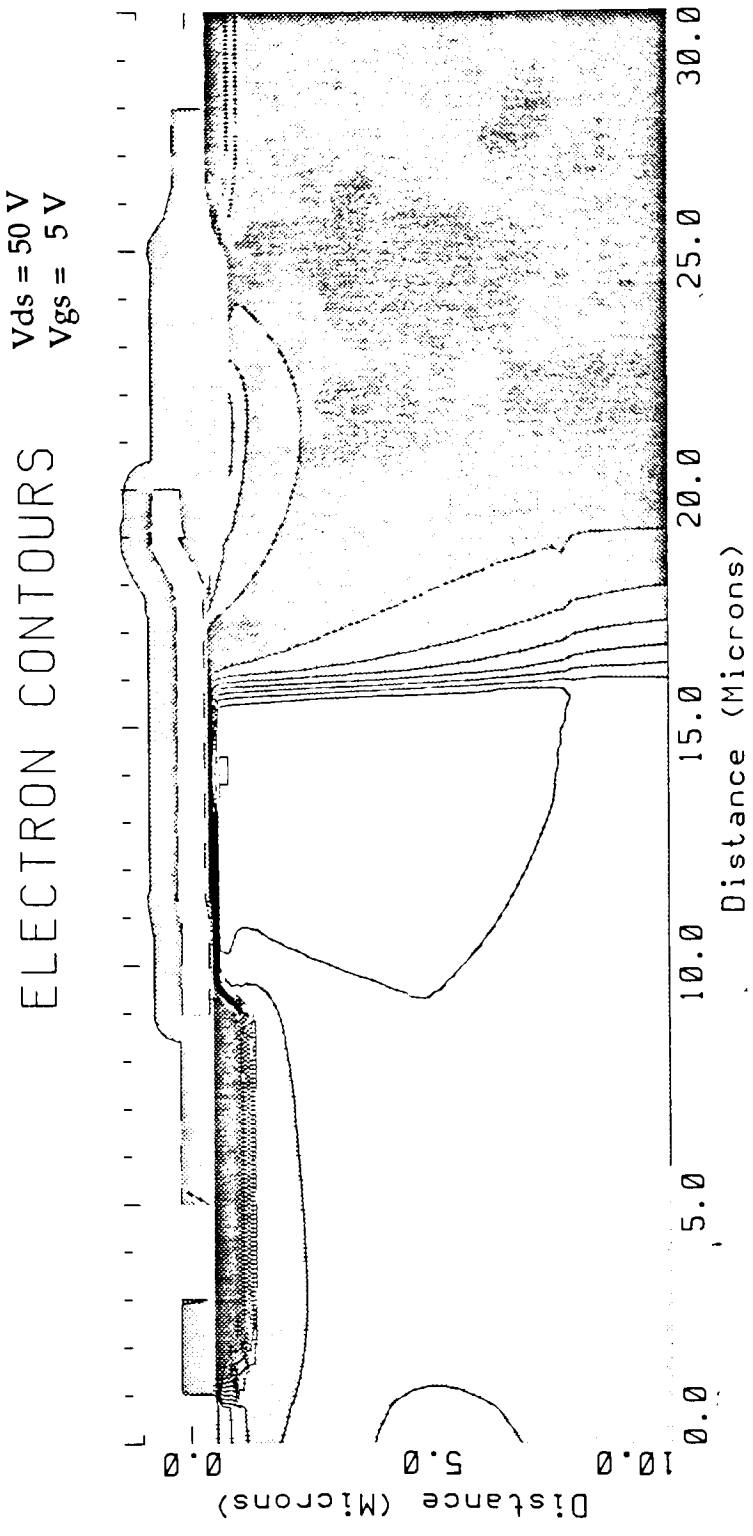
Potential contours with Vds = 50V and Vgs = 5V; (Contours = 2V/div.)

Fig 3.7



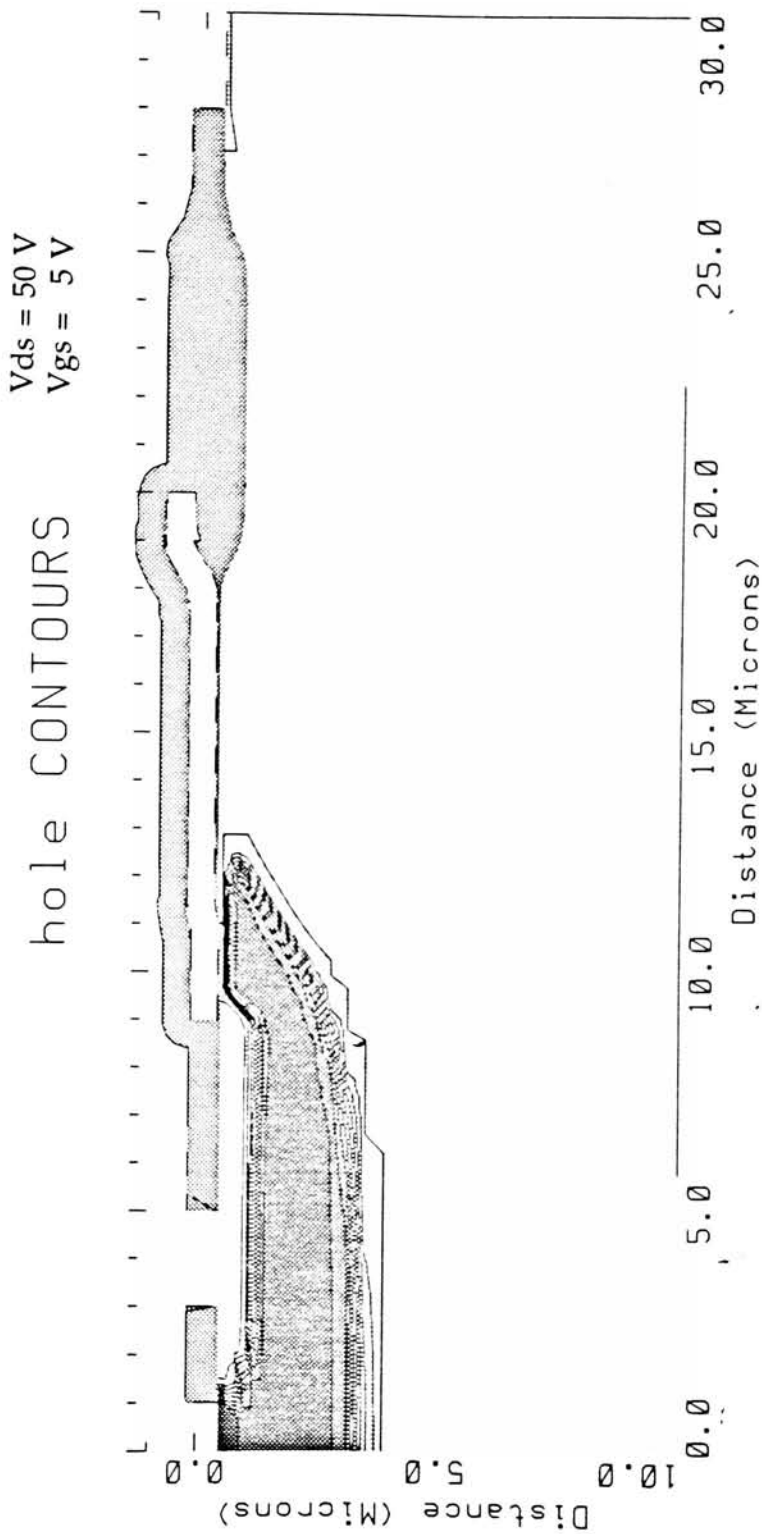
Current at 18μm showing effect of FOX forcing a buried channel

Fig 3.8



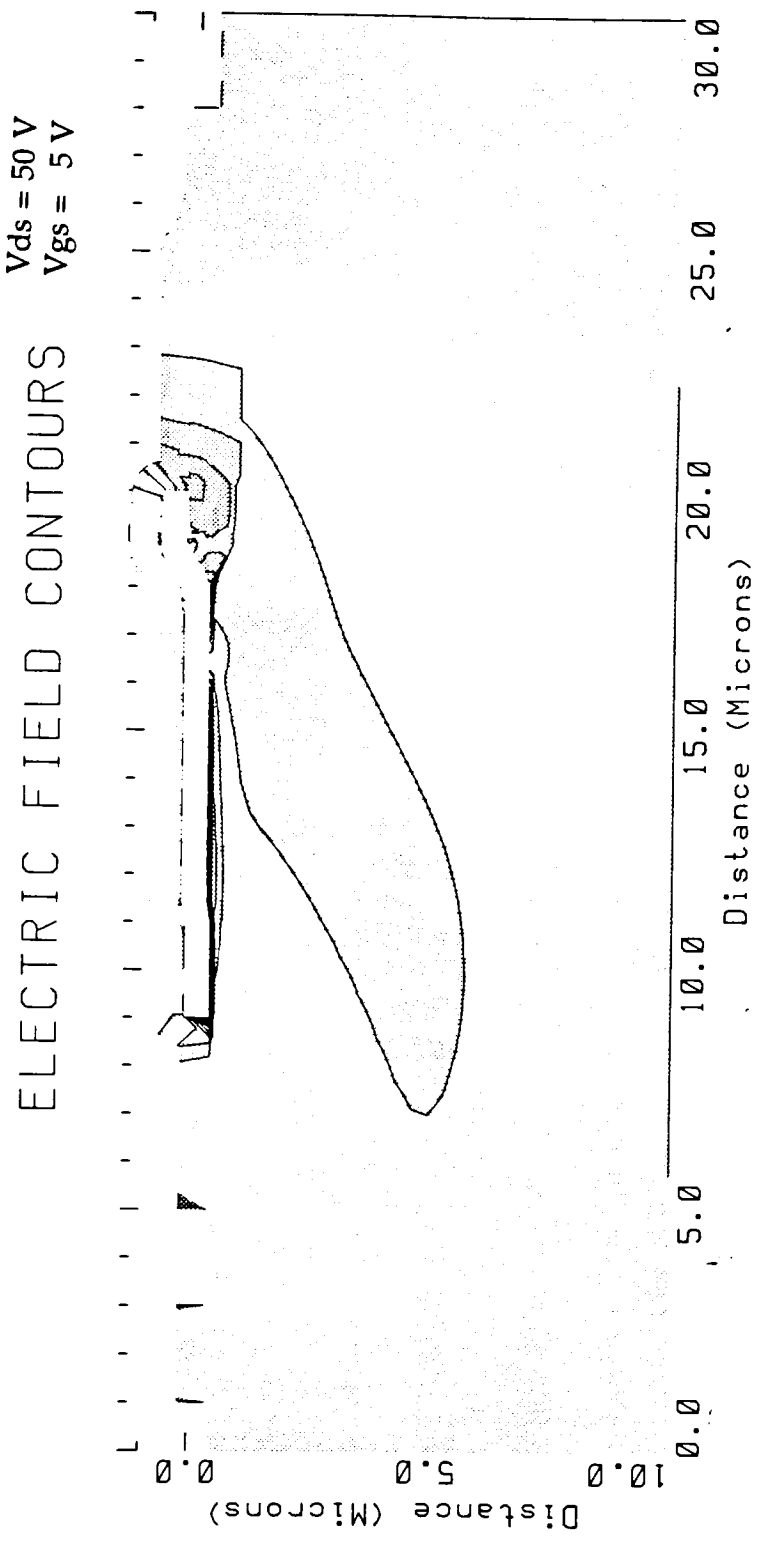
Electron contour for Vds = 50V and Vgs = 5V

Fig 3.9



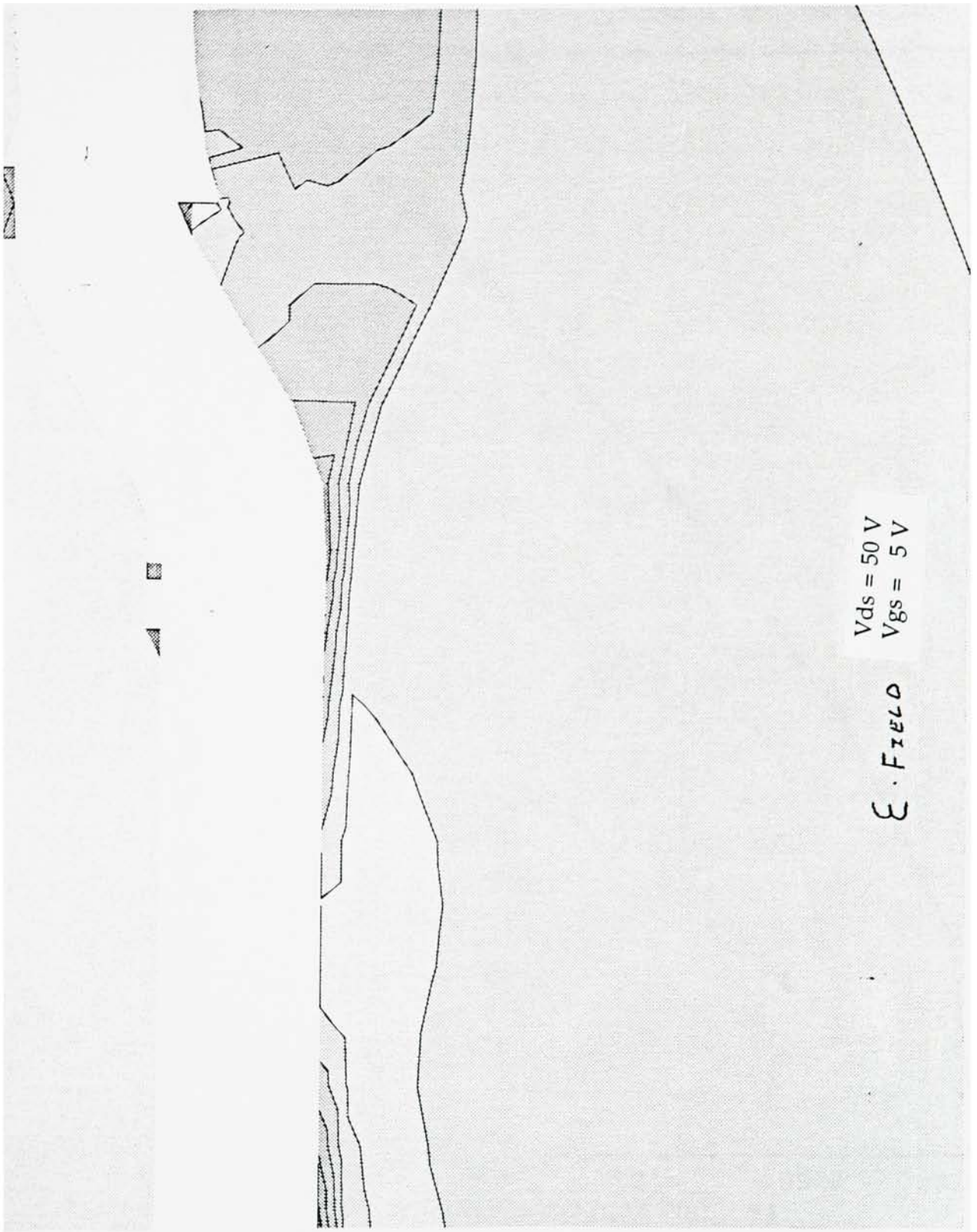
Hole contours for Vds = 50V and Vgs = 5V

Fig 3.10



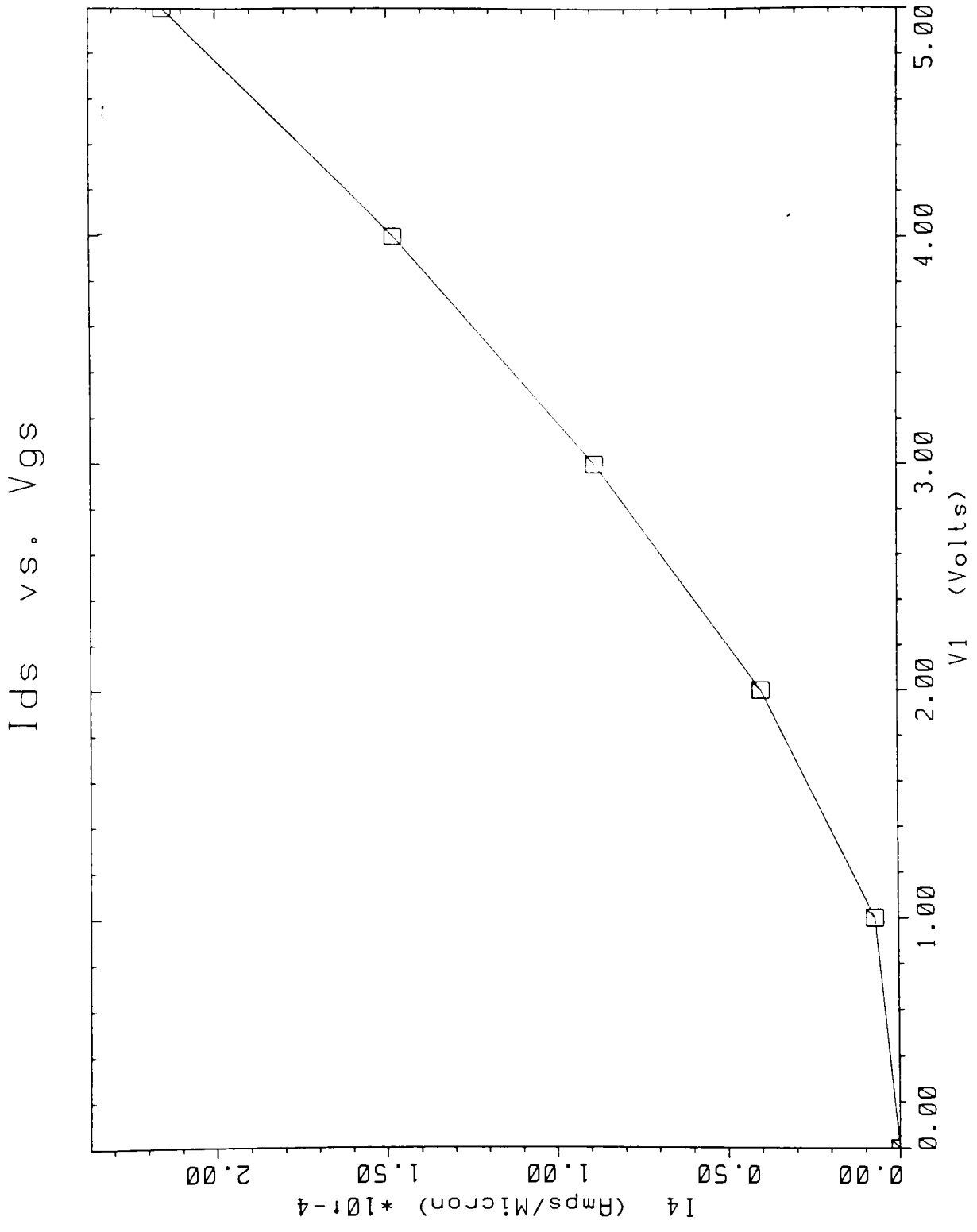
Electric Field contours for Vds = 50V and Vgs = 5V

Fig 3.11



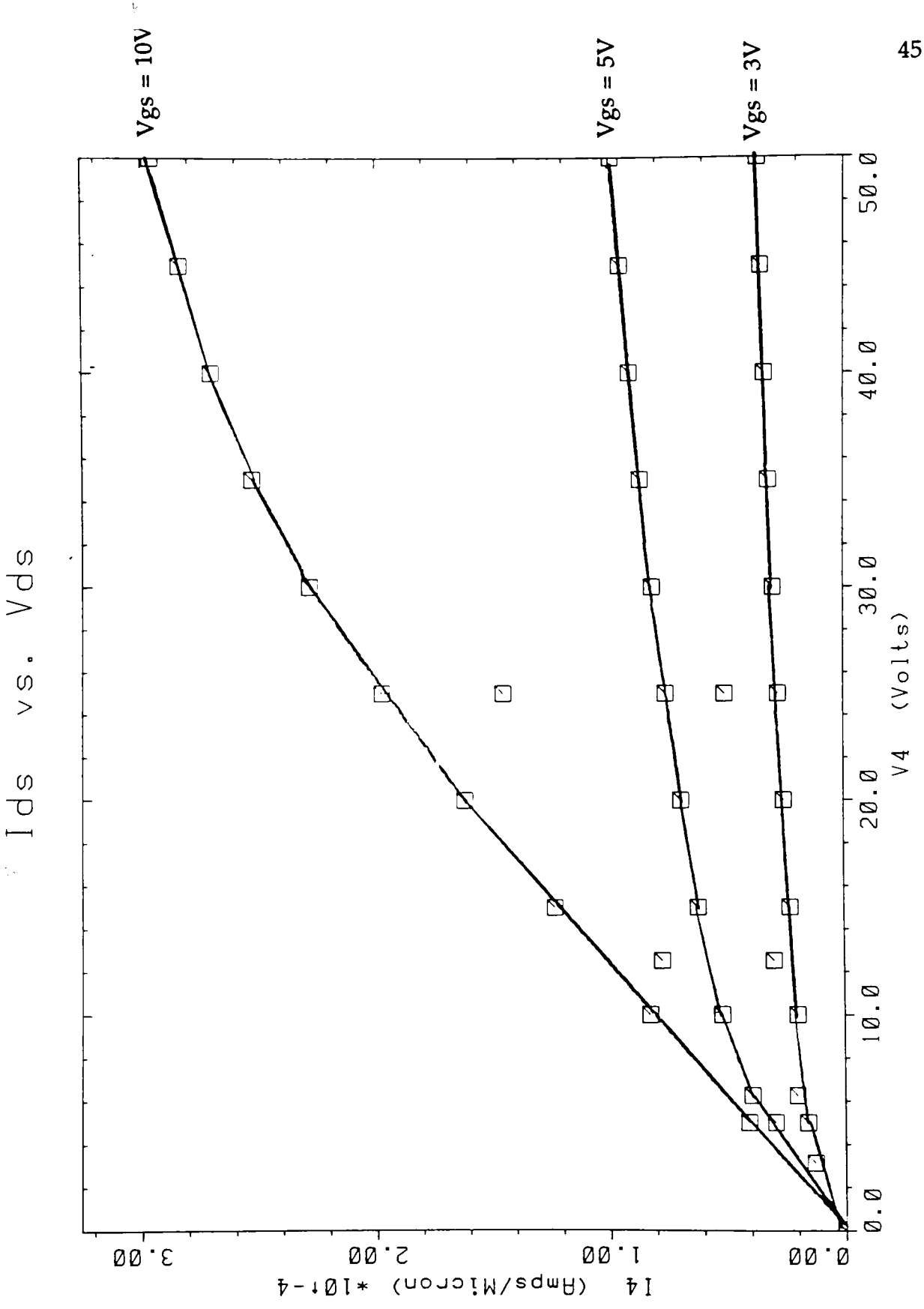
Close-up of electric field contours at expect breakdown point

Fig 3.12



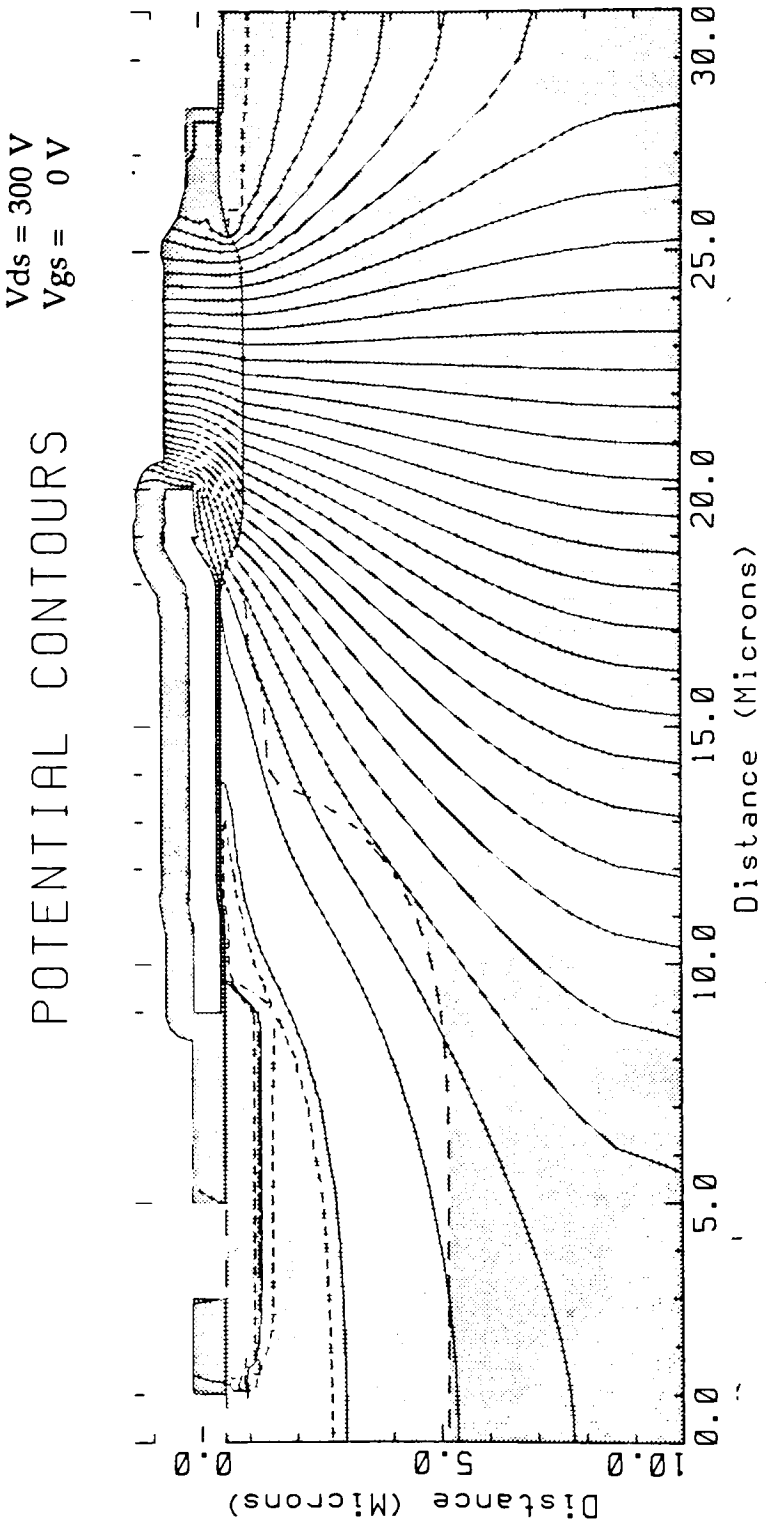
MEDICI simulation of Ids vs. Vgs for Power MOSFET

Fig 3.13



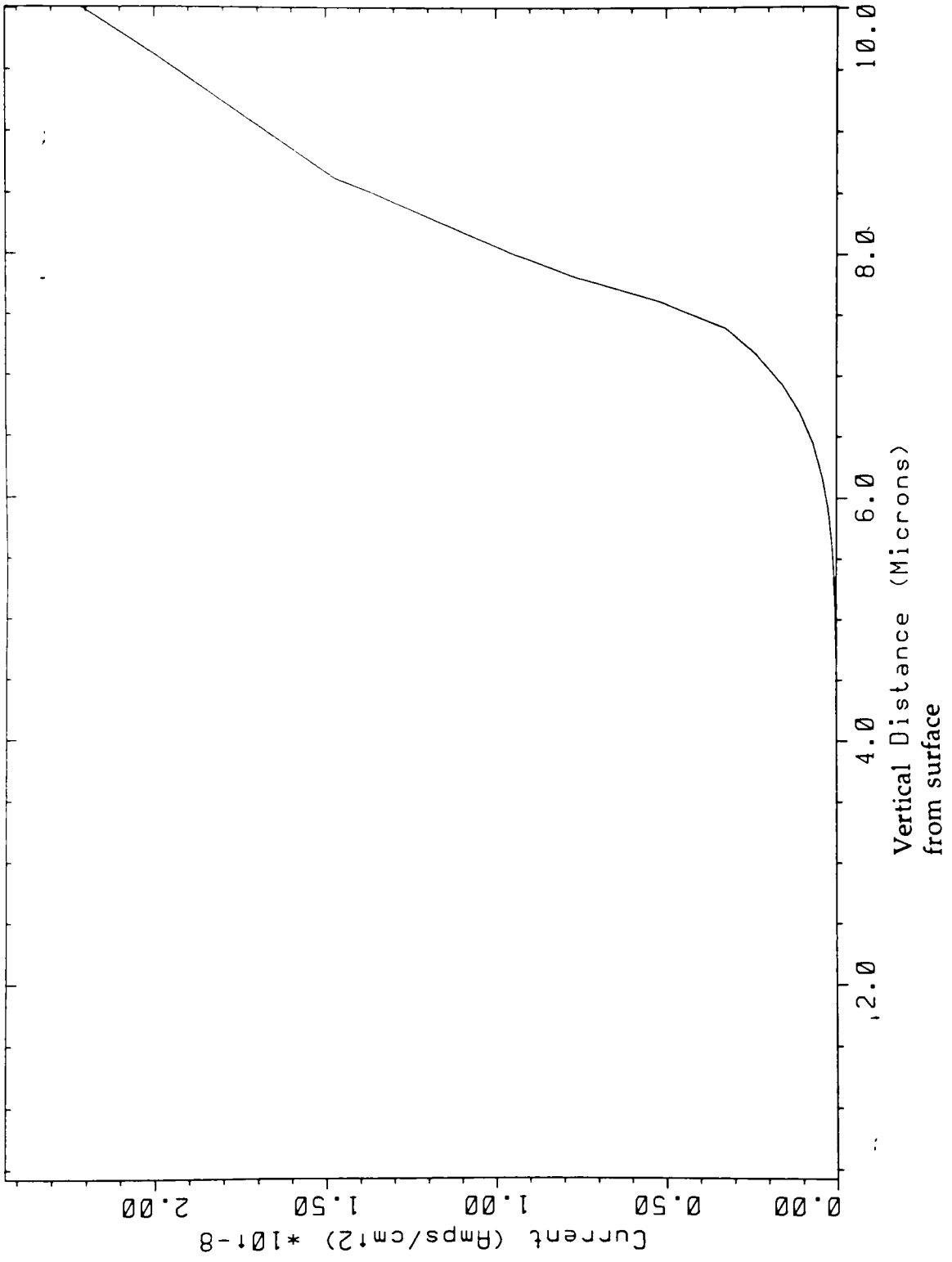
MEDICI simulation of Ids vs. Vds at select Vgs; Vdsmax = 50V

Fig 3.14



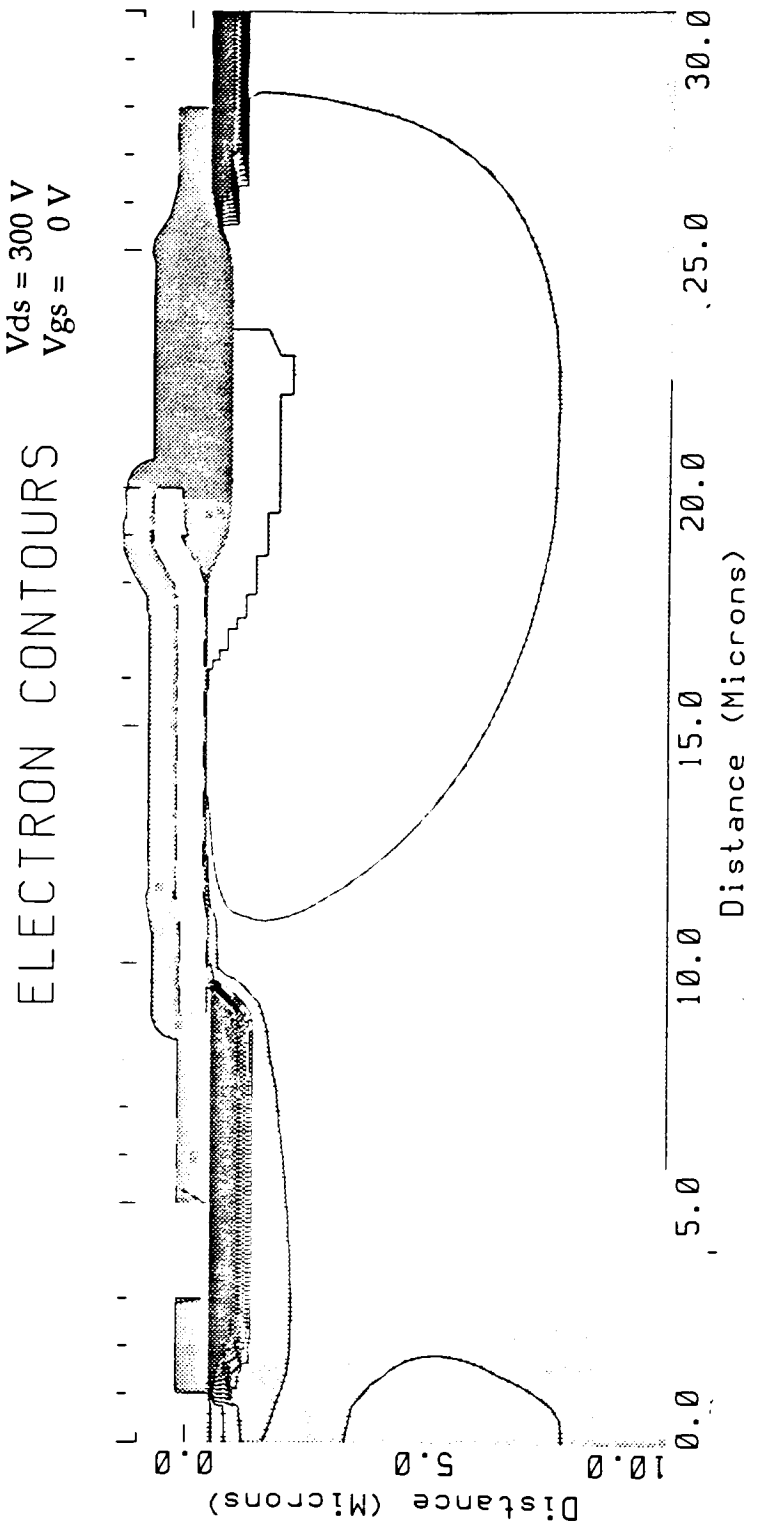
Potential contours for Vds = 300V and Vgs = 0V; (Contours = 10V/div.)

Fig 3.15



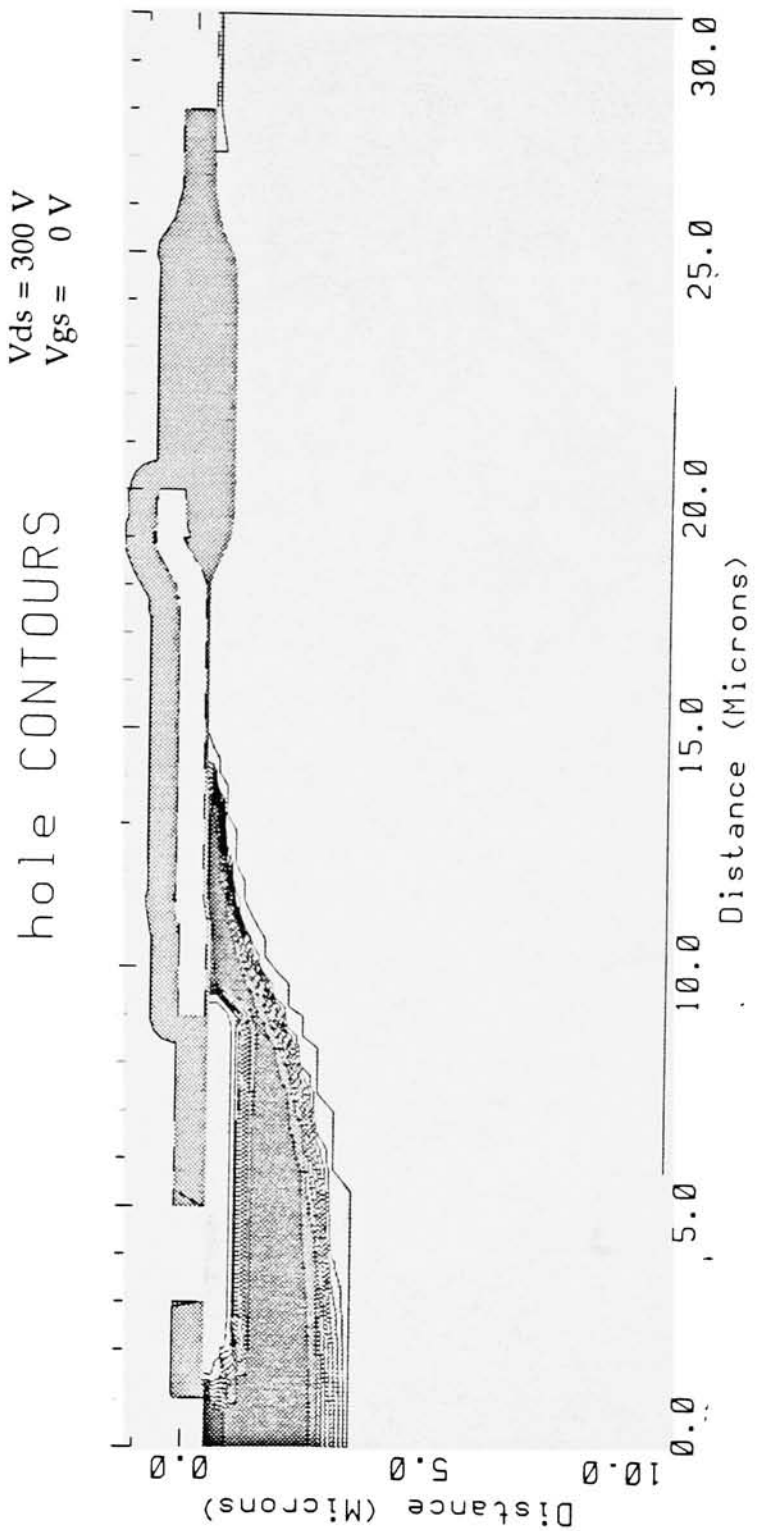
Current at 18μm showing negligible current flow or off state

Fig 3.16



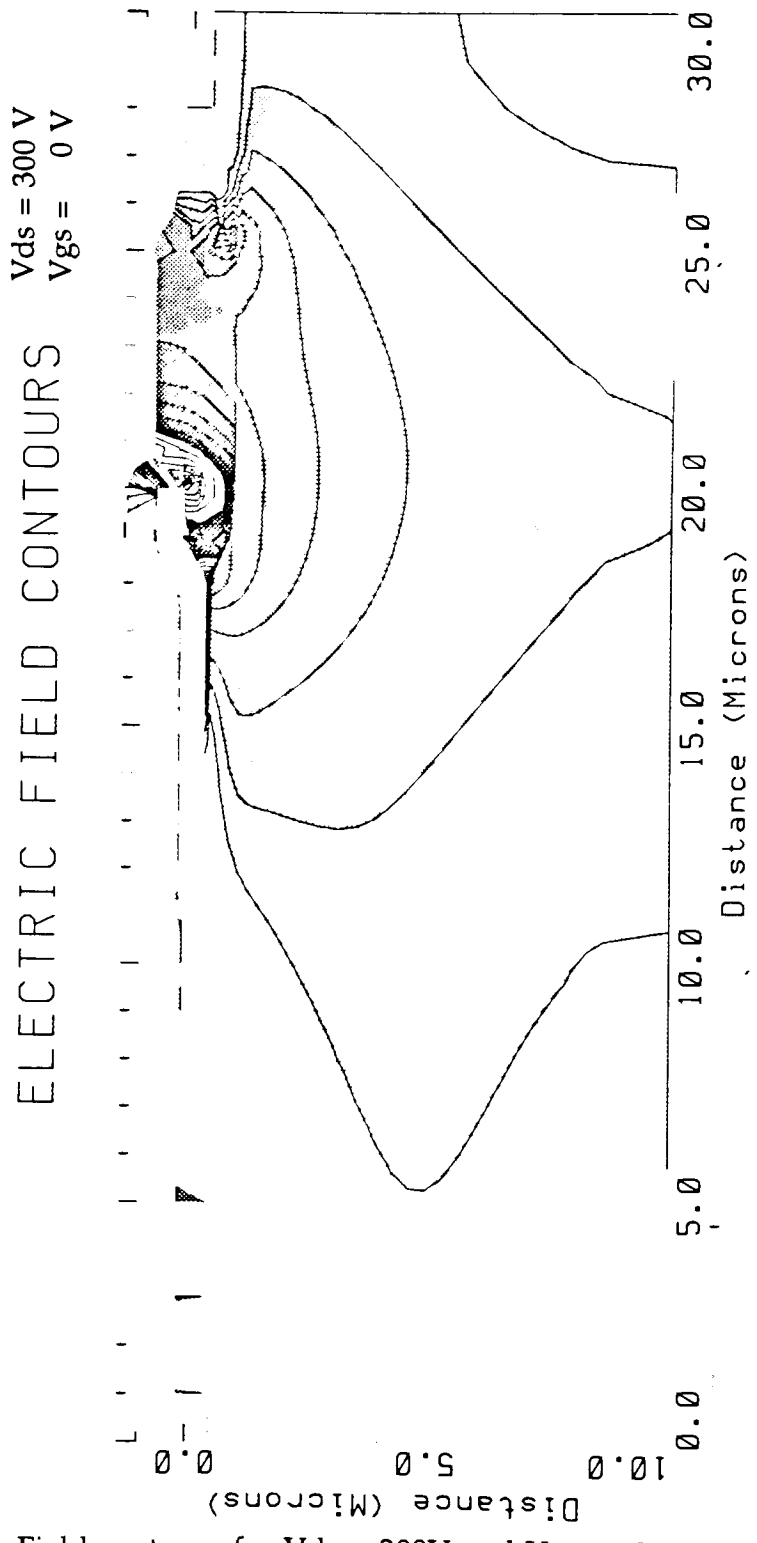
Electron contours for Vds = 300V and Vgs = 0V

Fig 3.17



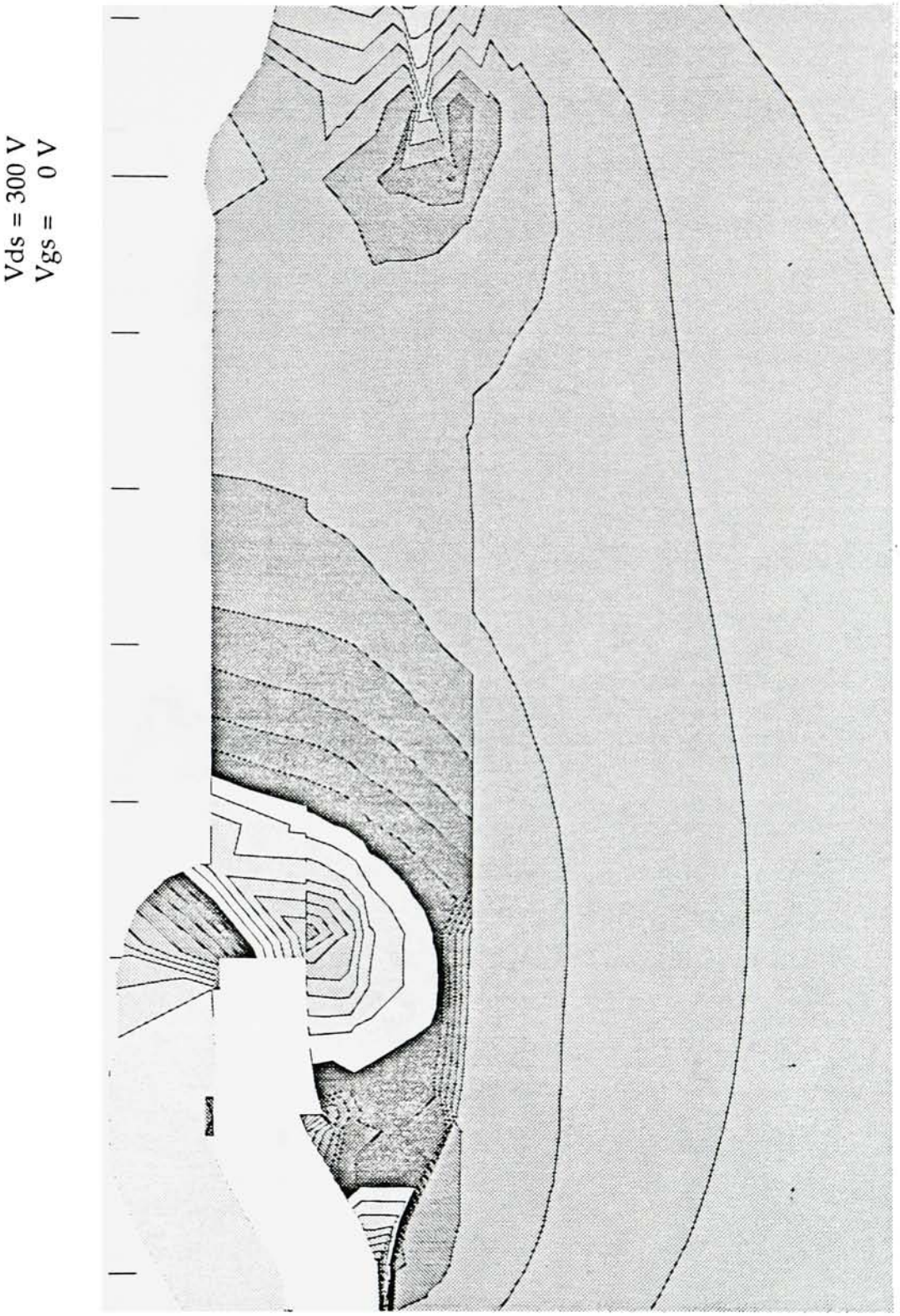
Hole contours for Vds = 300V and Vgs = 0V showing no channel formation

Fig 3.18



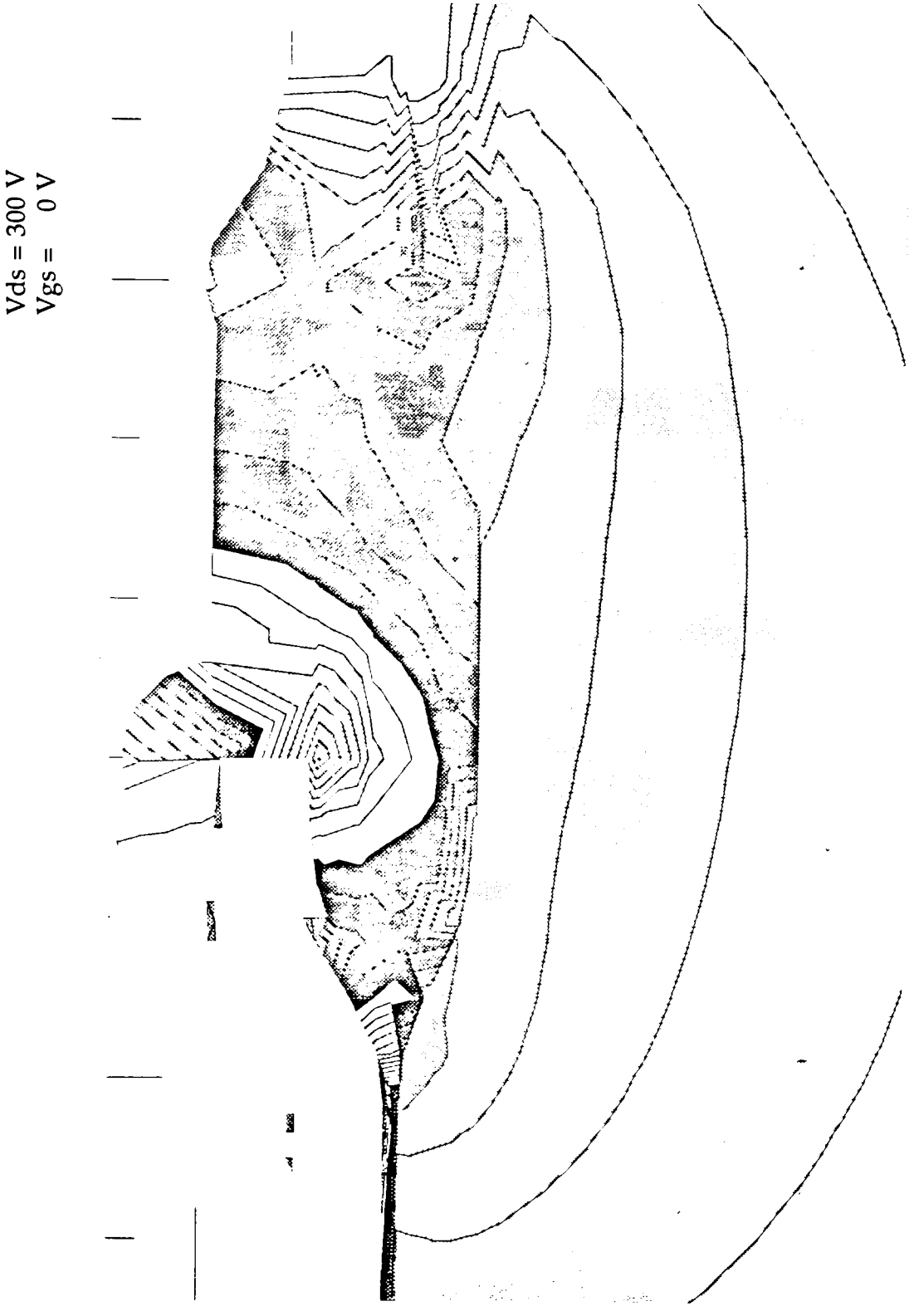
Electric Field contours for Vds = 300V and Vgs = 0V

Fig 3.19



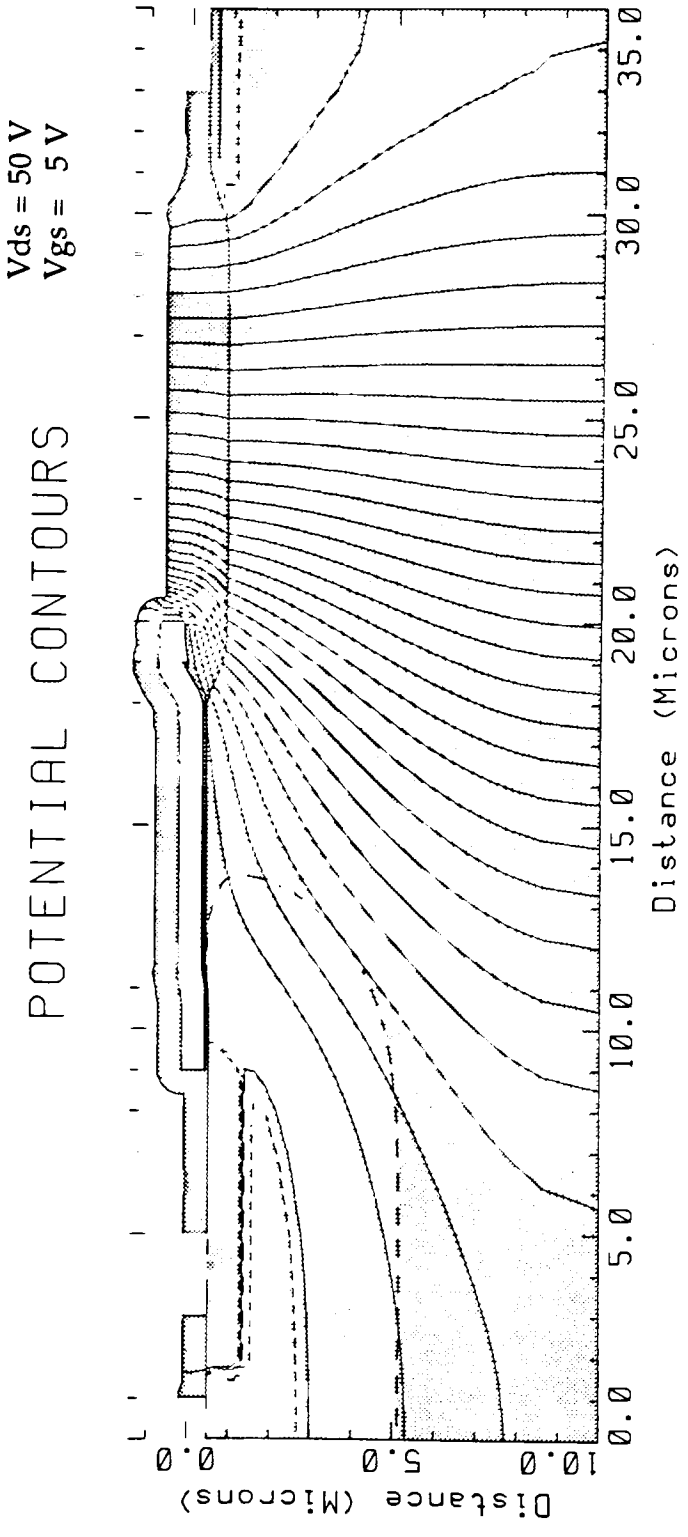
Close-up of electric field contours for shorter field plate overlap

Fig 3.20



Close-up of electric field contours for longer field plate overlap

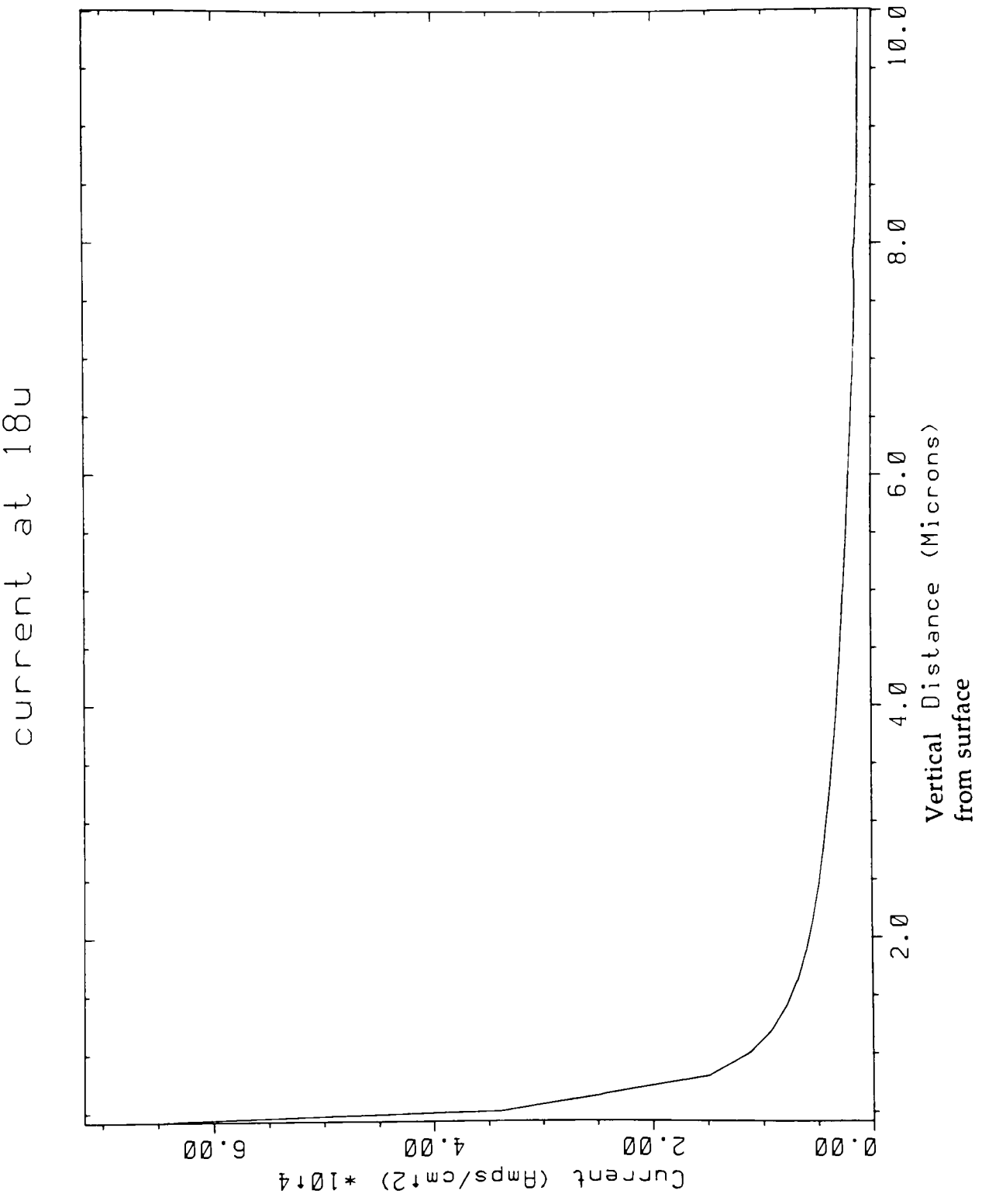
Fig 3.21



Potential contours for Vds = 50V and Vgs = 5V; (Contour = 2V/div.);

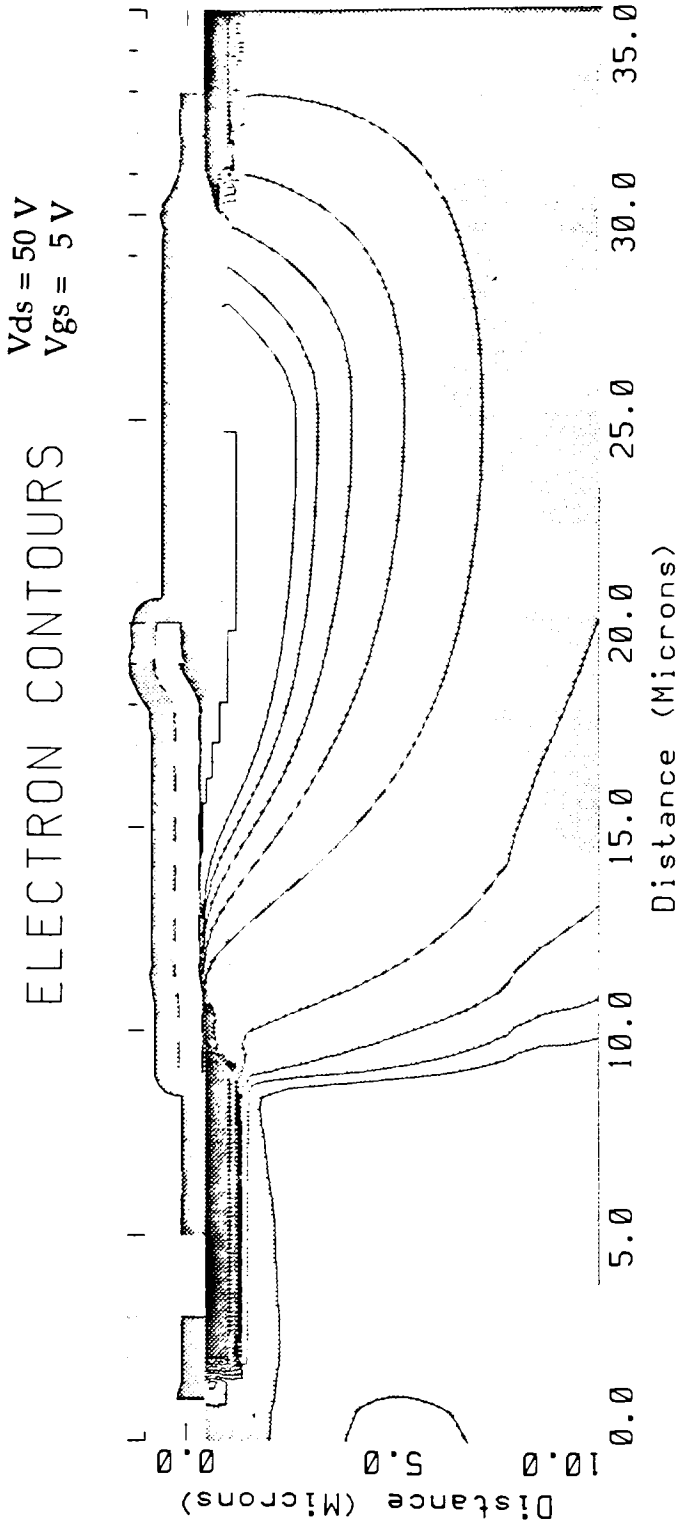
Corrected channel doping and increased drift region length device

Fig 3.22



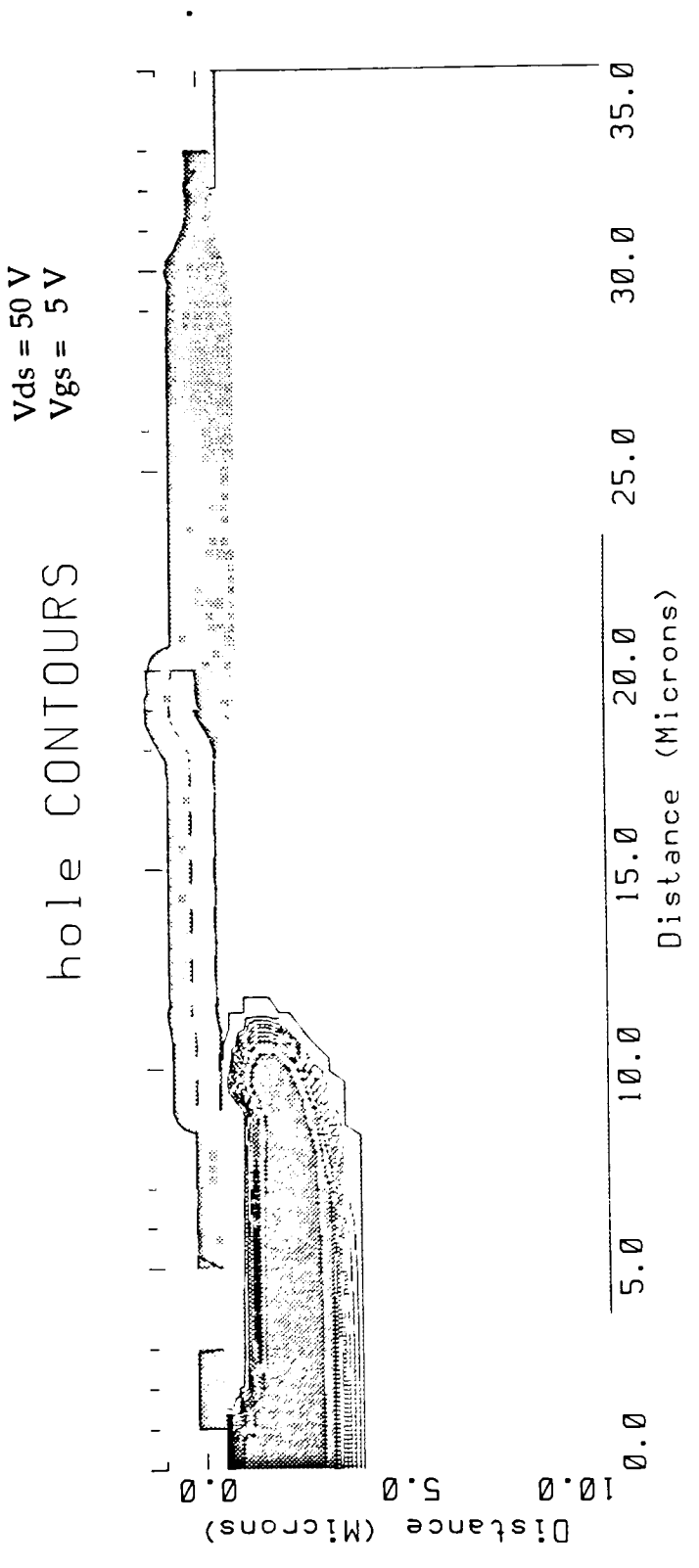
Current at 18μm showing effect of increased drift region length

Fig 3.23



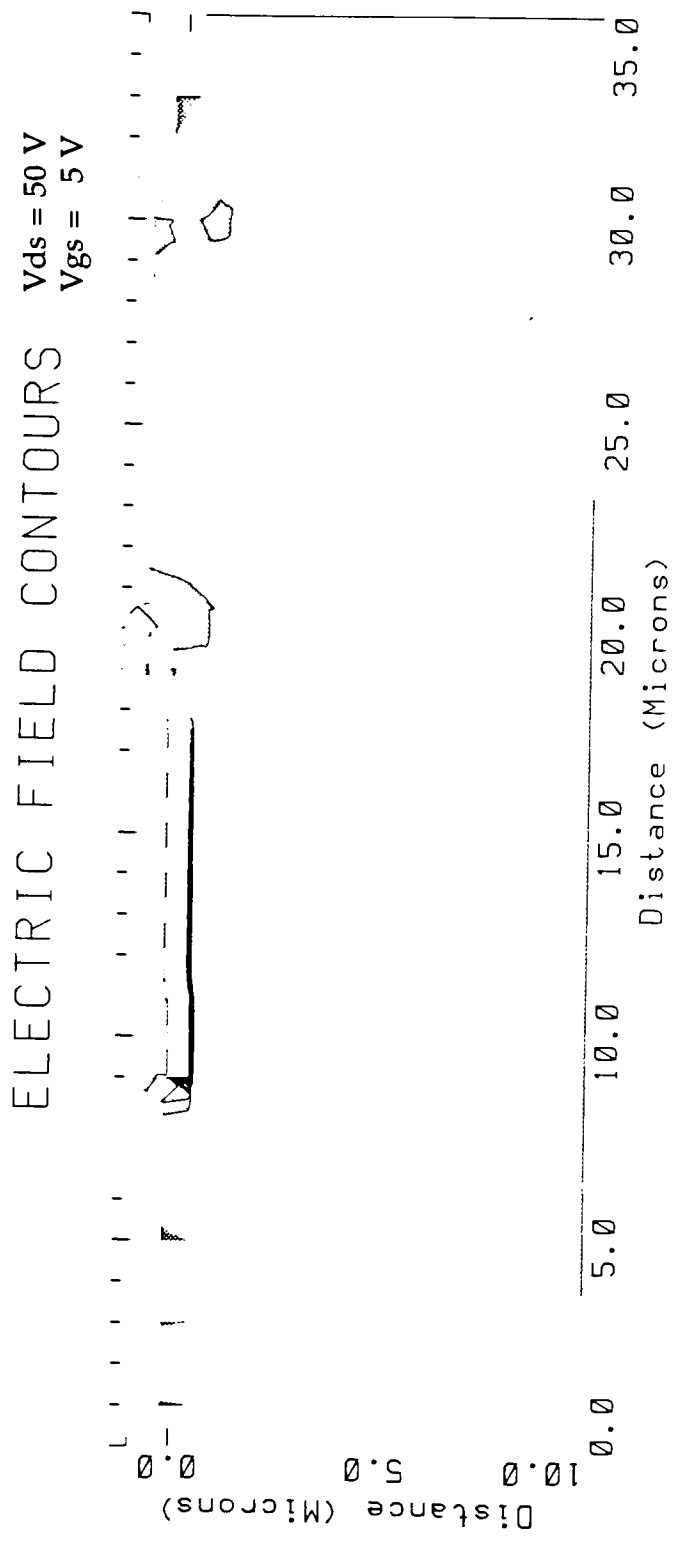
Electron contours for Vds = 50V and Vgs = 5V; Modified device

Fig 3.24



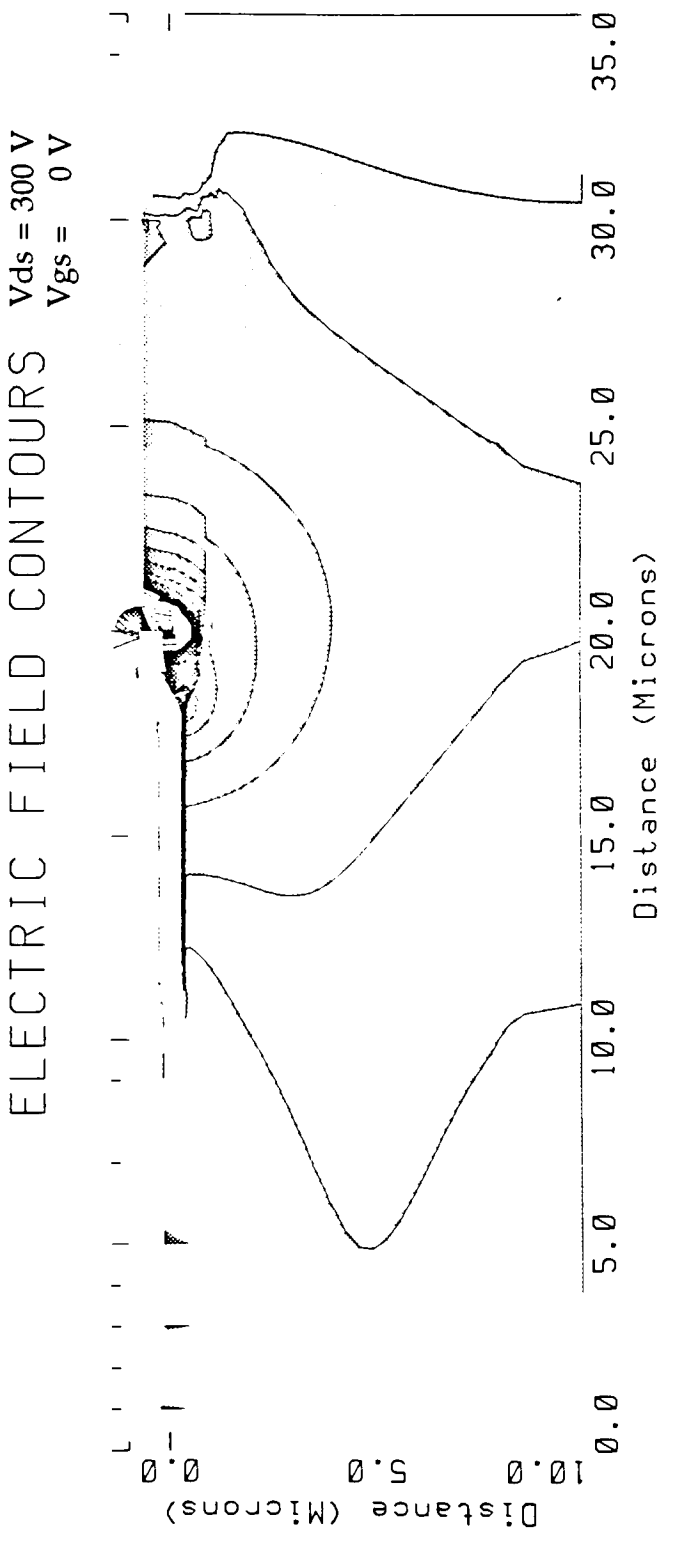
Hole Contours for Vds = 50V and Vgs = 5V; Modified device

Fig 3.25



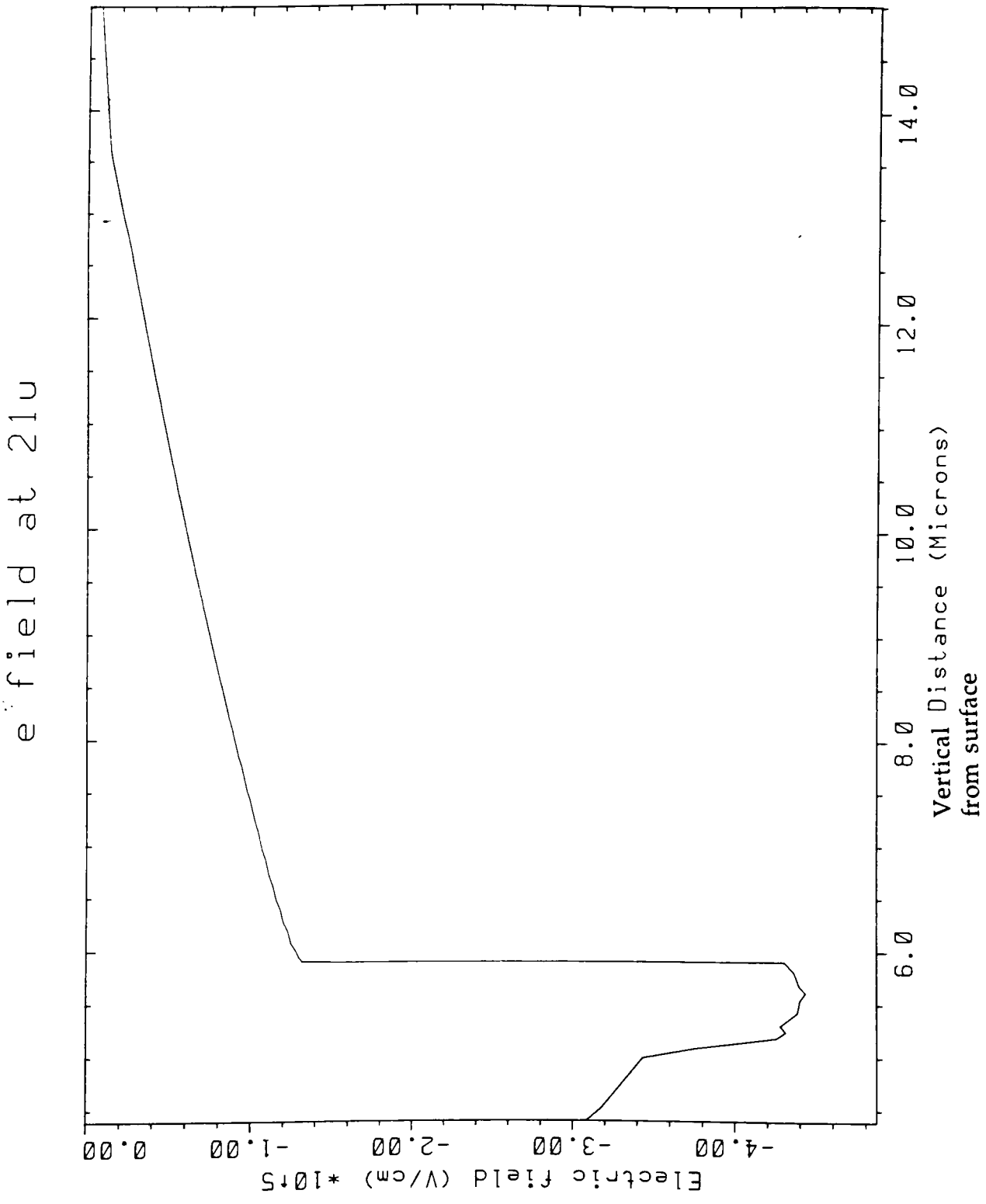
Electric Field contours for Vds = 50V and Vgs = 5V; Modified device

Fig 3.26



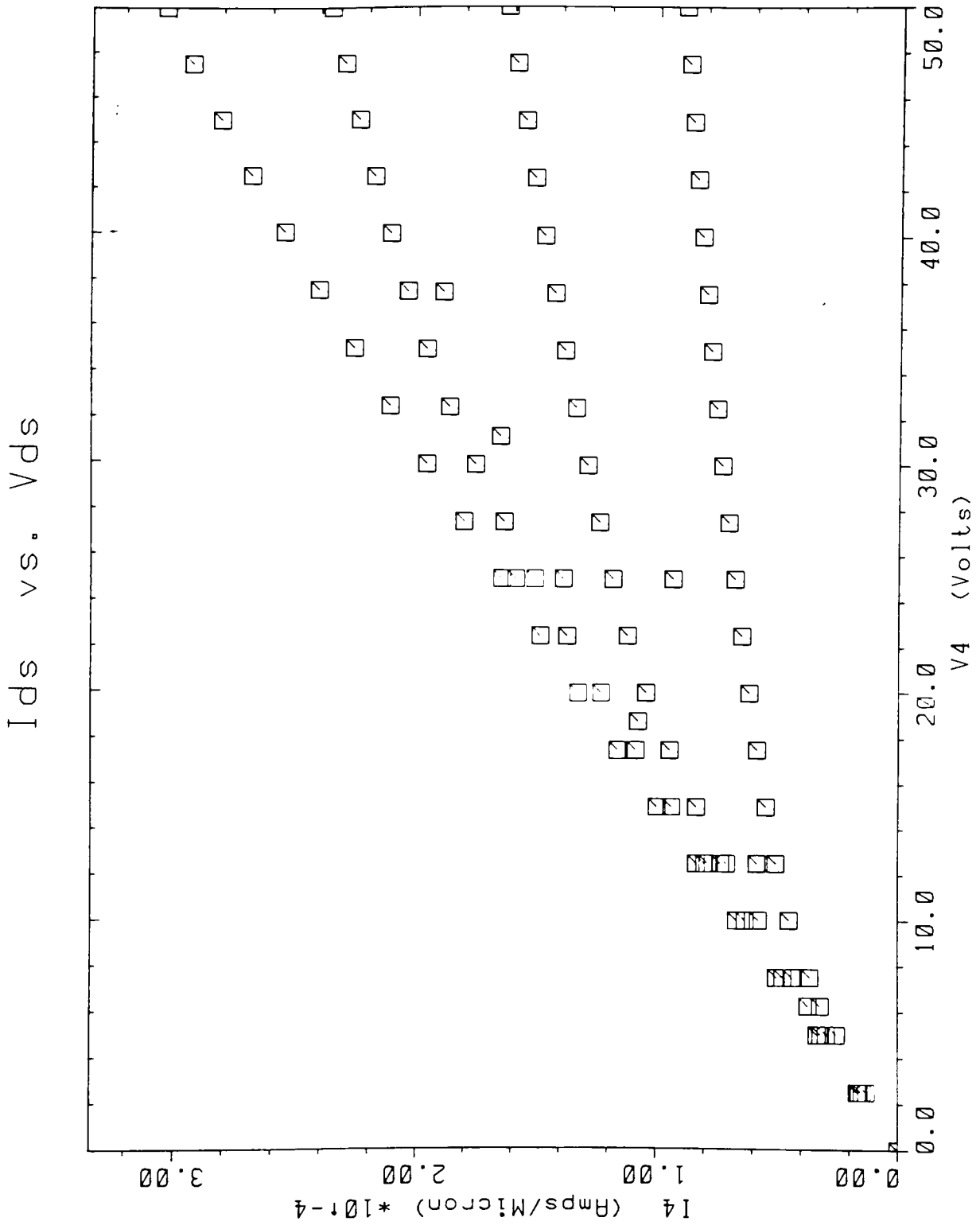
Electric Field contours for Vds = 300V and Vgs = 0V; Modified device

Fig 3.27



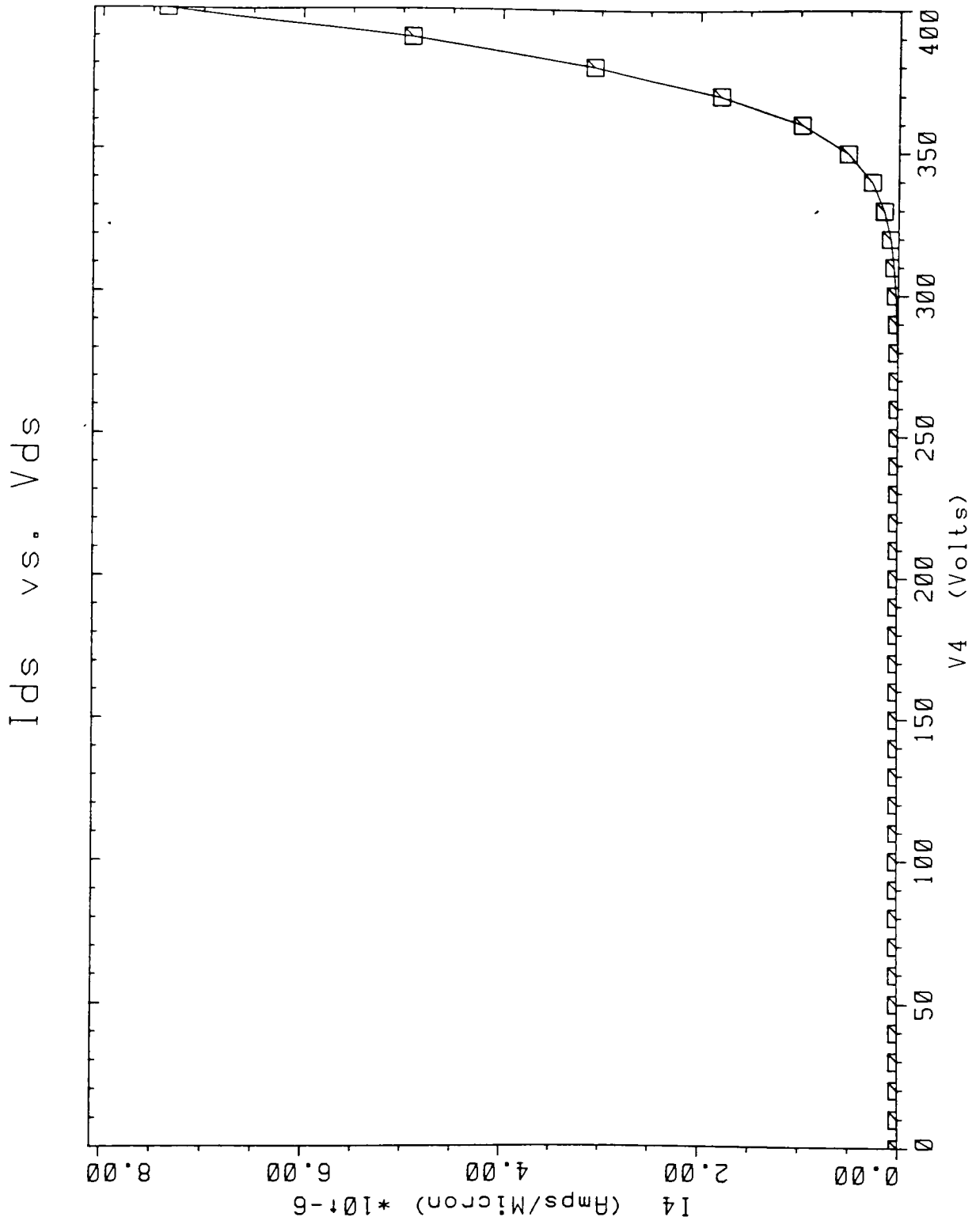
Electric field along a vertical line at 21μm, high field point; modified device

Fig 3.28



MEDICI simulation of Ids vs. Vds for modified device showing increased resistance

Fig 3.29



MEDICI simulation of breakdown voltage for fabricated device

Fig 3.30

3.3 Design Layout

The device layout for the power MOSFET and IGBT components was done using the Mentor Graphics IC Graph software on the Apollo workstations in the Computer Engineering Department's VLSI lab. A CIF file was created for the completed design and the file was then transferred to the fracturing software, CATS. It should be noted that the design rules for the layout were based on the Mosis Scalable and Generic CMOS design Rules, and a lambda of 2μm was used.

The design software is basically a polygon editing tool. For the design of high power devices, rounded corners are needed to reduce the harmful effects of the crowding of the electric field. This was achieved by typing : $set_mode(arc) when in the design window. This is not apparent in the software. This does not produce true arcs or circles. What is produced is a linear segment approximation. This results in some variation in the channel length around the corners.

The CMOS process definition file was initially used for the layout since the fabrication process is based on the CMOS process. For incorporation into future circuits an additional layer to mask the drift region of the power device from the Vt adjust implant should be added. Therefore a new process definition file was created for future power device designs and is called PWR_Design. It can be found in the directory RITPUB.

The layout includes three power MOSFET devices and three IGBT devices. A split to investigate the effects of varying the field plate overlap, FPO, was performed. The splits are shown in Table 3.2.1

Device	FPO (μm)	FOX (μm)
MOS #1	3	7
MOS #2	4	6
MOS #3	5	5
IGBT #1	3	7
IGBT #2	4	6
IGBT #3	5	5

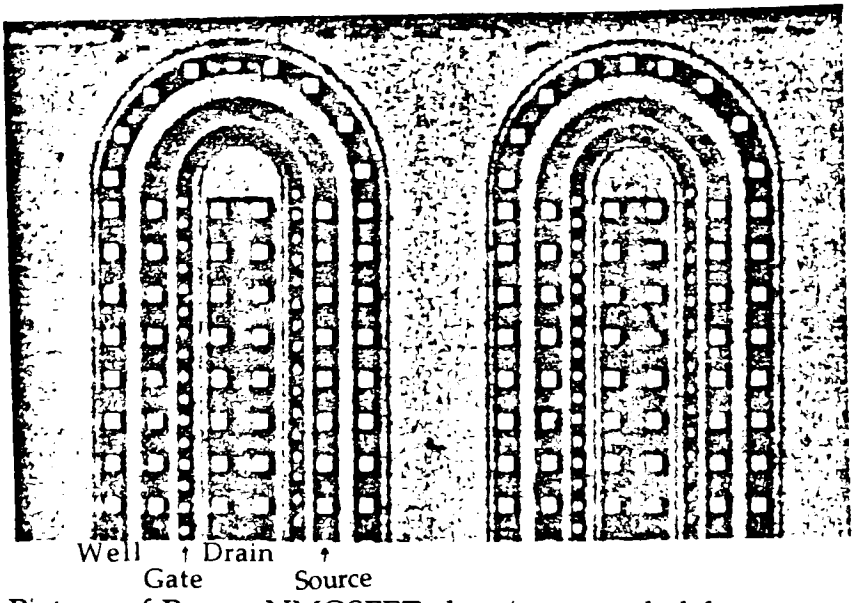
Table 3.2.1

When designing the devices special care must be taken to achieve the proper amount of lateral diffusion since this defines the dimensions and the doping of the channel region. The length of the drift region was kept constant at 10μ, while the FPO was varied.

The contact cuts to the well, source and drain were 10μm by 10μm. This provided a 10μm buffer around the contact cut. The contact cut to the poly was 5μm by 5μm and allowed for only a 3μm alignment tolerance.

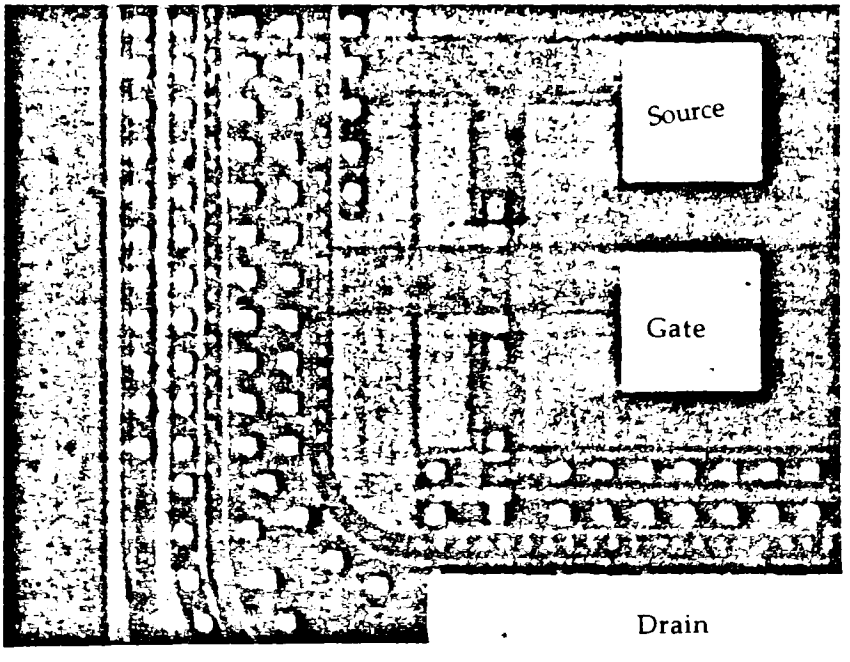
After initial testing, a Spin-on- Glass passivation layer was added and a VIA mask level was needed. The VIA cuts were large and made only to the original probe pads. This was done to reduce the amount of drain to gate to source exposure. All of the layers are displayed in Appendix C. Fig 3.31 and

Fig 3.32 show the actual device after fabrication and the curves used to reduce the electric field.



Picture of Power NMOSFET showing rounded features

Fig 3.31



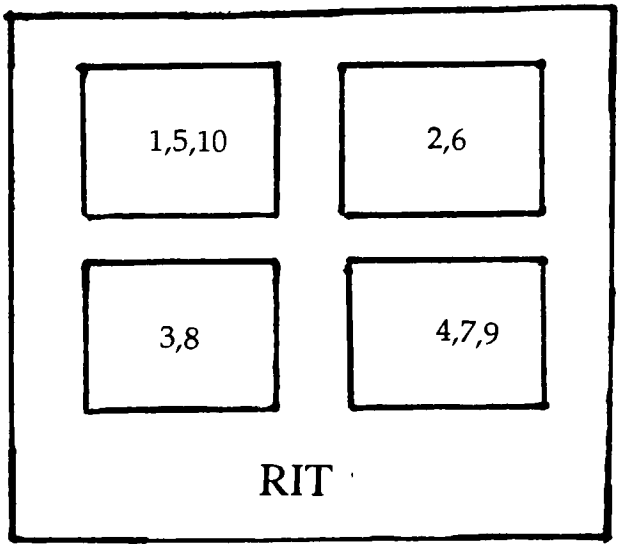
Picture of Power NMOSFET showing rounded features; contact region

Fig 3.32

4. Fabrication

4.1 Mask Making

The masks for this project were produced on the MEBES I electron beam system. The system writes the pattern to resist coated 5x stepper reticles that are used to fabricate the device. Due to the number of levels needed for the design, four levels were written to each reticle to reduce the cost. Levels 1, 2, 3 and 4 are found on reticle 1; level 5, 6, 8 and 9 are found on reticle 2 and level 10 is found on reticle 3. Fig 4.1 shows the arraignment of the levels on the reticle.



Picture showing mask position on quartz stepper plate

Fig 4.1

In order to produce the mask levels, the table (Table 4.1) indicates the conversion from I.C. Station levels to reticle levels. The clear or dark field mask indicates if the area of interest is to be protected or exposed. Dark exposes an area while clear protects. Note that R.I.T. uses positive resist in its CMOS process.

IC Level	IC Name	Reticle Level	Reticle Name	Dark or Clear Field Mask
1*	N Well	-------	-------	----------
2	P Well	1	Well	Dark
3	Active	2	Active	Clear
4	N+ Select	6	N+ S/D	Dark
5	P+ Select	4 and 7***	Vt Adj	Clear
			P+ S/D	Clear
6	Poly	5	Poly	Clear
7	Contact_A	8**	CC	Dark
8	Contact_P	8**	CC	Dark
9	Metal	9	Metal	Clear
10	Via	10	Via	Dark

* The IC Level 1 is not used in this design
** IC Levels 7 and 8 are 'ORed' together to produce the Reticle Level 8
*** For this process the Reticle levels 4 and 7 are identical

Table 4.1

This table was the initial conversion from IC to mask levels. Changes have been made to improve the process and this table is presented in the discussion section.

The stepper job NEWCMOS.FAC, found in the [10,1] directory of the GCA Stepper, was written to execute a separate pass for each of the four positions on the reticule. This program was also written for two different reticules to be exposed on the same wafer without overlap. This allows for a test chip and device chip to be fabricated simultaneously. The key offsets and shifts have been determined and entered into the job deck. A second alignment mark was provided in case the original one became hard to see. In order to use the second alignment mark, the shift must be corrected in the original stepper job deck. Levels 1, 5, and 10 use pass 1; levels 2 and 6 use pass

2; levels 3 and 8 use pass 3 and levels 4 and 9 use pass 4. To expose two reticles, the letters T or D are to follow the pass number to indicate which chip is being exposed. An example may be: 1T, 2D meaning pass 1 of reticule T(est) and pass 2 of reticule D(evice).

4.2 Device Processing

This section describes the process steps for the fabrication of the two lateral power devices (LDMOS and IGBT). Device cross sections at various stages of the process are provided. The process technology for the power devices were based on the already existing RIT P-well CMOS process. These steps are listed below. Deviations from the standard RIT P-well CMOS process are shown in bold type. Specific details of the processing steps as well as the control wafer data is provided in Appendix D.

The fabrication lot consisted of five device wafers and seven control wafers. The device wafers and the first six control wafers were N type wafers with a resistivity of 5 - 15 Ω-cm. Control wafer number seven was a P type wafer with a resistivity of 10 - 20 Ω-cm. The wafers were scribed for identification and four point probed to determine the specific resistivity of each.

The wafers then received a Modified RCA clean. The mixture for this clean was 1:1:5, H2O2 to HCl to water, for the HPM, a 50:1 DI to Hf mix for the oxide etch and 1:3:15, NaOH to H2O2 to water, for the APM. The clean was administered as such: 10 min. HPM, 5min DI water rinse, 1min Oxide Etch,

5min DI water rinse, 10min APM, 8min DI water rinse. The DI water rinses were not to exceed 10min at any point in the process. By reducing the concentration of the NaOH, a smoother surface is be obtained and particles are not overoxidized. Also, the alkaline APM is more effective at removing particles. By placing it last in the clean, more particles generated in other steps are removed and a cleaner surface is achieved.

The alignment oxide was then grown. This oxidation was at 1100C for 35min and resulted in a 0.5μm oxide thickness, see Fig. 4.2 for cross section.

The well region was then patterned with resist and the oxide was etched in BOE. With the photoresist left on to mask the oxide, the p-well implant of B11 was done at a dose of 4e12 and an energy of 50 KeV. The photoresist was stripped off and the wafers were cleaned in the Modified RCA clean. The well implant was then driven in at a temperature of 1125C. The first 240min were in dry O2 to make a step for future alignment purposes and the next 960min were in N2 for the drive-in. This is shown in Fig. 4.3.

At this point all of the oxide was removed. The control wafer was checked to ensure that the proper implant and junction depth was achieved. A pad oxide of thickness 1000Å was deposited at 1100C for 50min in dry O2. A layer of CVD nitride was then deposited. A thickness of 1500Å was obtained in 10min at 810C. The cross section for this is in Fig. 4.4.

The oxide and nitride layers were then patterned with photoresist to be the negative of the active area desired. The exposed nitride and oxide were

etched. The photoresist was then removed. The cross section for this in shown in Fig. 4.5.

The channel stop photolithography was then done. The power device does not require this so the resist protected the entire device for the implant. The wafers were then implanted with B11 at a dose of 8e13 and an energy of 100KeV. The resist was stripped and the wafers were cleaned. A field oxide of 10,000Å was grown at 1100C in wet O2 for 210min. This is shown in Fig. 4.6.

With the field oxide grown, the control wafer was again checked to see the effects of the thermal step on the junction depth of the well. The nitride and pad oxide were etched off and the wafers were cleaned in the Modified RCA clean. The resulting active area in shown in Fig. 4.7.

The KOOI oxide was then grown to a thickness of 1000Å in 900C of wet O2 for 45min. A blanket implant of B11, dose of 5.3e11 and energy of 60KeV, was performed for the PMOS Vt Adjust. The wafers were then coated in resist and the NMOS Vt Adjust photolithography was done. This was done so that only the NMOS were affected by the next implant. This method allows the CMOS to be matched and also the desired threshold voltage magnitude is achieved for both NMOS and PMOS. This is shown in Fig. 4.8. An implant of B11, dose of 4e12 and energy of 60 KeV, was then performed.

The photoresist was than removed and the KOOI oxide was etched off. The wafers were then cleaned in the Modified RCA clean. The cross section showing in Fig. 4.9 shows the boron doping profile.

The gate oxide of the device was then grown at 1100C in dry O2 for 35min to obtain a thickness of 1000Å. The control wafers were again checked to see the effects on the well junction and to ensure that the threshold adjusts were correct. This is shown in Fig. 4.10.

A layer of polysilicon was then deposited to form the gate electrode. The poly layer was doped with phosphorus spin on dopant glass. The spin on glass was then removed after a 25min 900C drive in step. The control was then probed to ensure sufficient doping. Care must be taken not to dope the substrate through the gate oxide. (25) This is shown in Fig 4.11.

The poly was then patterned with photoresist and the exposed poly was then etched in a RIE tool. The photoresist was then removed. Again all resist strips were done with acetone or nanostrip if possible. This was to reduce possible damage to the gate structure. The cross section of the poly gate is shown in Fig 4.12.

The P+ areas on the device were then patterned. For the power MOSFET the well contact was the only area to receive the P+ implant. For the IGBT device the drain region also received the P+ implant. These cross sections are shown in Fig 4.13 and Fig 4.14 respectively.

With the P+ implant areas patterned, the gate oxide in these areas was etched off and an implant of BF2 with a dose of 4e15 and 120 KeV was performed. The resulting boron concentrations shown in Fig 4.15 for the MOSFET and FIG 4.16 for the IGBT were obtained.

The N+ areas on the device were patterned. Again the MOSFET and IGBT required different implant areas. The cross sections are shown in Fig 4.17 and Fig 4.18 respectively.

The devices then received an implant of phosphorous with a dose of 4e15 and en energy of 150KeV. The increase in energy was needed to implant deeper into the silicon so that the drain of the MOSFET was not isolated by the boron threshold adjust implants. The photoresist was stripped and the resulting phosphorous concentrations were achieved (see Fig 4.19 for the MOSFET and Fig 4.20 for the IGBT). The last two control wafers were then checked to determine the junction depths of the P+ and N+ implants and also the concentration of the implants.

A layer of undoped spin on glass was applied to act as a passivation layer. The contact cuts to the well, source, drain and gate were then patterned and the spin on glass was etched. The photoresist was then removed. The relevant cross section is shown in Fig. 4.21.

The wafers were then cleaned and a 8000Å thick layer of aluminum was sputtered on the devices. The aluminum film was then patterned and etched to form the electrode connections. The photoresist was removed and the wafers were sintered at 415C in a N2/H2 mixture for 20min. The final device cross sections are presented in Fig 4.22 for the MOSFET and Fig 4.23 for the IGBT.

After initial testing a surface leakage problem was encountered, another layer of spin on glass was applied and via cuts were patterned and

etched so that contacts to the pads could be made and increased isolation provided. To perform the oxide etch on aluminum, a new etch chemical was needed since the standard HF etch would also etch the aluminum layer underneath. A glycerin and HF mixture was used. The mixture was 3:1 Buffered HF to glycerin. A series of oxide on aluminum wafers were etched to determine the etch time and the selectivity of the etch. The exposure of the etch mixture to water did increase the aluminum etch rate; therefore care must be taken during the etch and rinse steps to avoid damage to the aluminum pads. (23) Larger dimensions showed less damage than smaller ones due to the ability of the rinse to clear the area of the mixture before reacting and etching the aluminum film.

Outline of P-well CMOS process steps:

1. Scribe: (100), 5 15 Ohm-cm, N-Type
2. 4 pt Probe
3. **Modified RCA Clean**
4. Photo Oxide: Xox = 5000Å, Time=35 min., Temp=1100C in Wet O2
5. Photolith: Level 1 : P-Well
6. Etch Oxide: Buffered HF for 6 min
7. Implant: Type = Boron(B11), Dose = 4e12, Energy = 50KeV
8. **Wet strip Photoresist**
9. **Modified RCA Clean**
10. Well Drive: Xox=2840Å, Time=240 min., Temp=1125C in Dry O2
    Time=960 min., Temp=1125C in N2

11. Etch Oxide: All

c 12. Groove: For Xj

c 13. 4 pt Probe

14. Pad Oxide: Xox = 1000Å, Time = 50 min., Temp = 1100C
in Dry O2

15. CVD Nitride: Xni = 1500Å, Time = 10 min., Temp = 810C

16. Photolith: Level 2 : Active Area

17. Etch Nitride:Plasma Etch

18. Etch Oxide: Buffered HF for 1.5 min.

19. **Wet Strip Photoresist**

20. Photolith: Level 3 : Channel Stop

21. Implant: Type:Boron(B11), Dose = 8e13, Energy = 100KeV

22. **Chemical Etch Photoresist**

23. **Modified RCA Clean**

24. Field Oxide: Xox = 10,000Å, Time = 210min, Temp = 1100C
in Wet O2

c 25. Groove: for Xj

26. Etch Nitride:Buffered HF for .5 min., Plasma Etch

27. Etch Oxide: Buffered HF for 1.5 min.

28. **Modified RCA Clean**

29. KOOI Oxide: Xox = 1000Å, Time = 45 min., Temp = 900C
in Wet O2

30. Implant: Type = Boron(B11), Dose = 5.3e11, Energy = 60 Kev

31. Photolith: Level 4 : NMOS - Vt Adjust

32. Implant Type = Boron(B11), Dose = 4e12, Energy = 60 Kev

33. **Wet Strip Photoresist**

34. Etch Oxide: Buffered HF for 1.5 min.

35. **Modified RCA Clean**

36. **Gate Oxide: Xox = 1000Å, Time = 35min, Temp = 1100C in Dry O2, Ramp up and Down in Dry O2**

c 37. Groove: for Xj

c 38. 4 pt Probe

39. CVD Poly: Xpoly = 6000Å

40. N-Type Diffusion: Spin-on Phosphorus Dopant

41. Etch Oxide: Buffered HF for .5 min.

c 42. 4 pt Probe

43. Photolith: Level 5 : Poly Gate

44. Etch Poly: RIE in SF6 + O2

45. **Wet Strip Photoresist**

46. Photolith: Level 6 : P+ Source/ Drain

47. Etch Oxide: Buffered HF for 1.5 min.

48. Implant: Type = Boron(BF2), Dose = 4e15, Energy = 120KeV

49. **Wet Strip Photoresist**

50. Photolith: Level 7 : N+ Source/ Drain

51. **Implant: Type=Phosphorus, Dose=4e15, Energy=125KeV**

52. **Wet Strip Photoresist**

53. SOG: Xsog = 6000Å RMP = 3000, Time = 30 sec
Anneal Temp. = 900C, Time = 20min.

c 54. Groove: for Xj

c 55. 4 pt Probe

56. Photolith: Level 8 : Contact Cuts

57. Etch Oxide: 8000Å of Spin-On-Glass in Buffered HF

58. **Wet Strip Photoresist**

59. **Modified RCA Clean**

60. Sputter Al : Pressure = 5mTorr, V = 340V, I= 10amps,
    Time = 18min.
61. Photolith: Level 9 : Metal
62. Etch Al: Temp=45C
63. **Wet Strip Photoresist**
64. Sinter: Time = 20min., Temp = 415C, Gas = H2/N2
65. **SOG: Xsog = 3000Å RMP = 3000, Time = 30sec**
66. **Photolith: Level 10 : VIA**
67. **Etch SOG: Use special etch to protect Al**
68. **Wet Strip Photoresist**
69. Test

Note: The c notation indicates that the step were performed on only the control wafers included in the lot.

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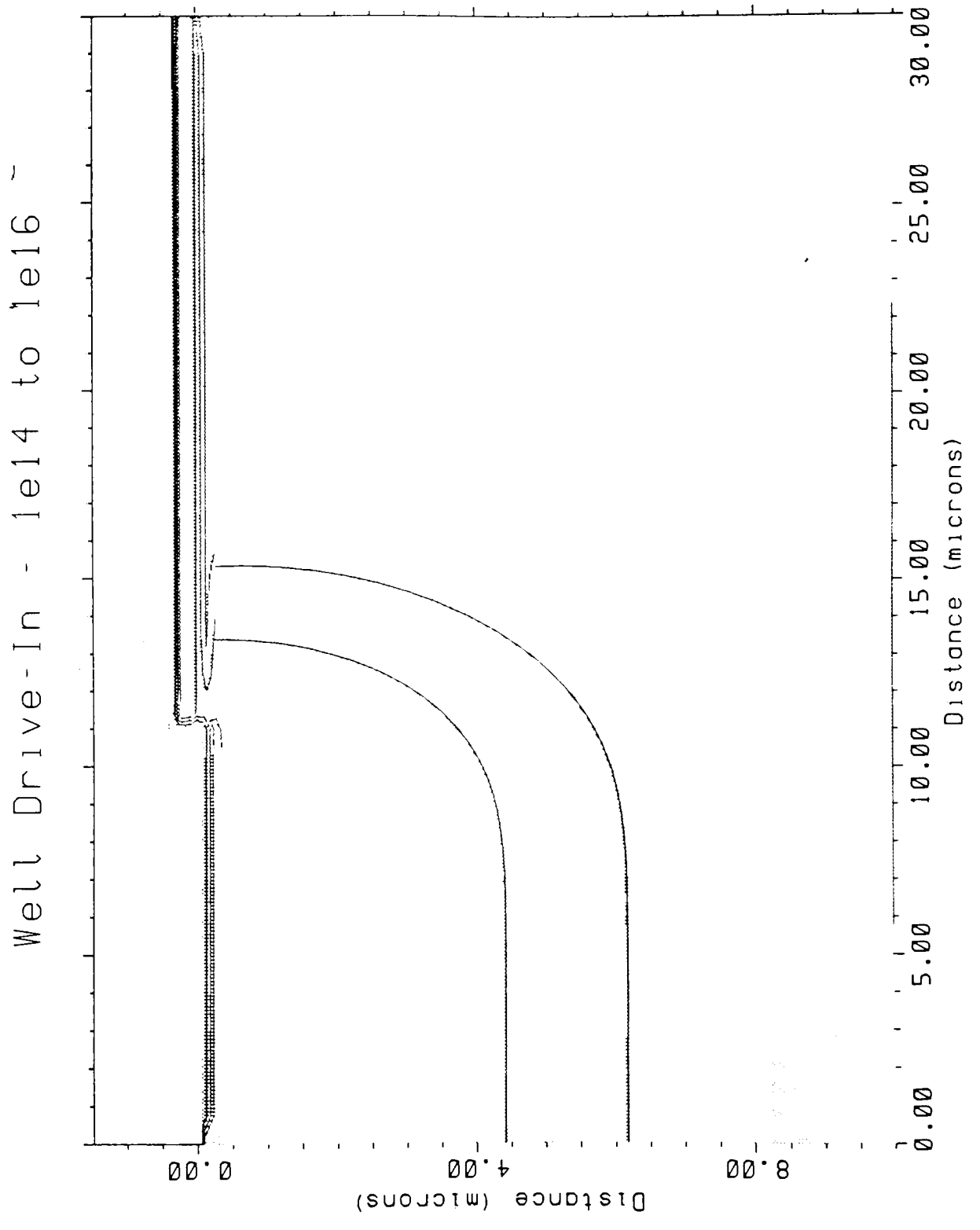
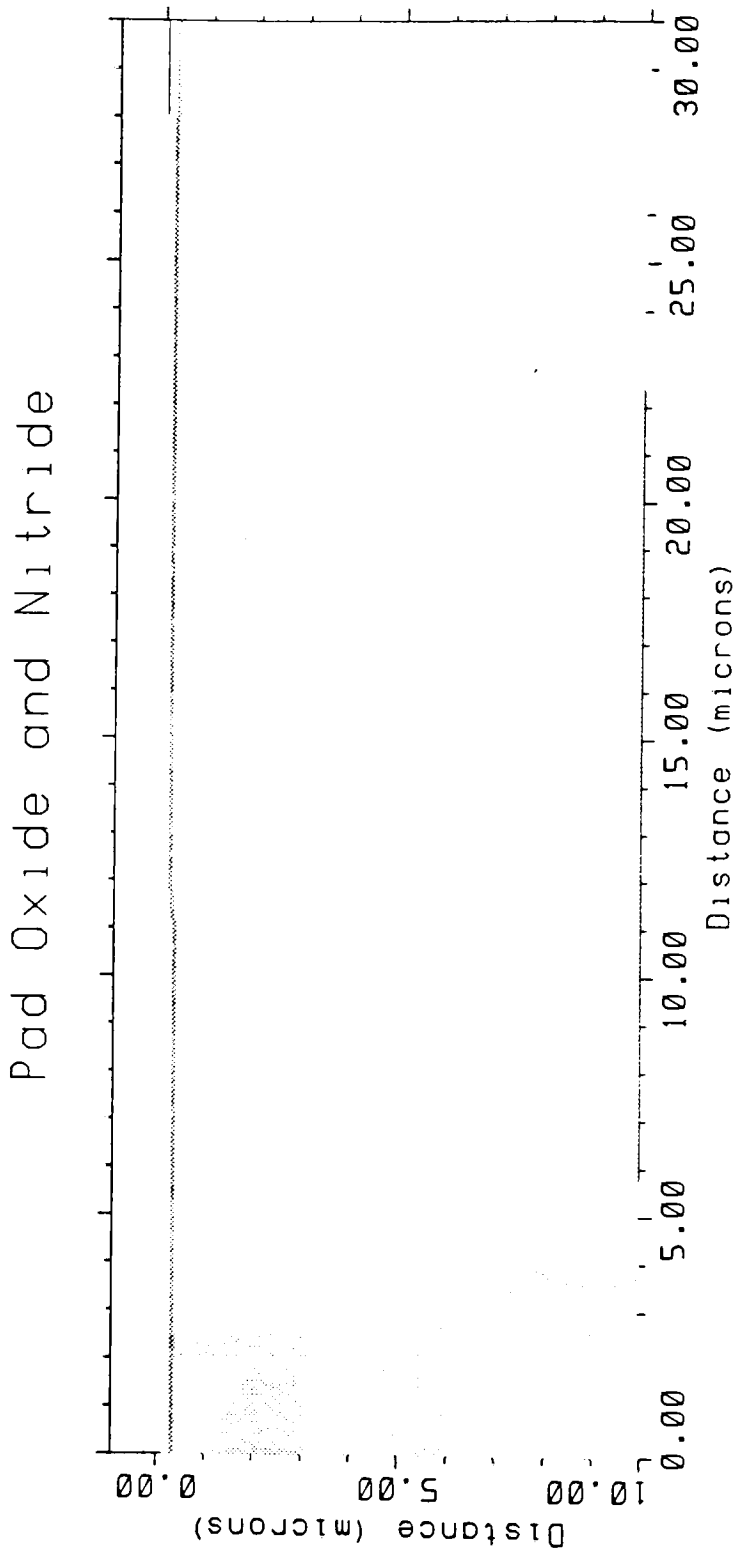


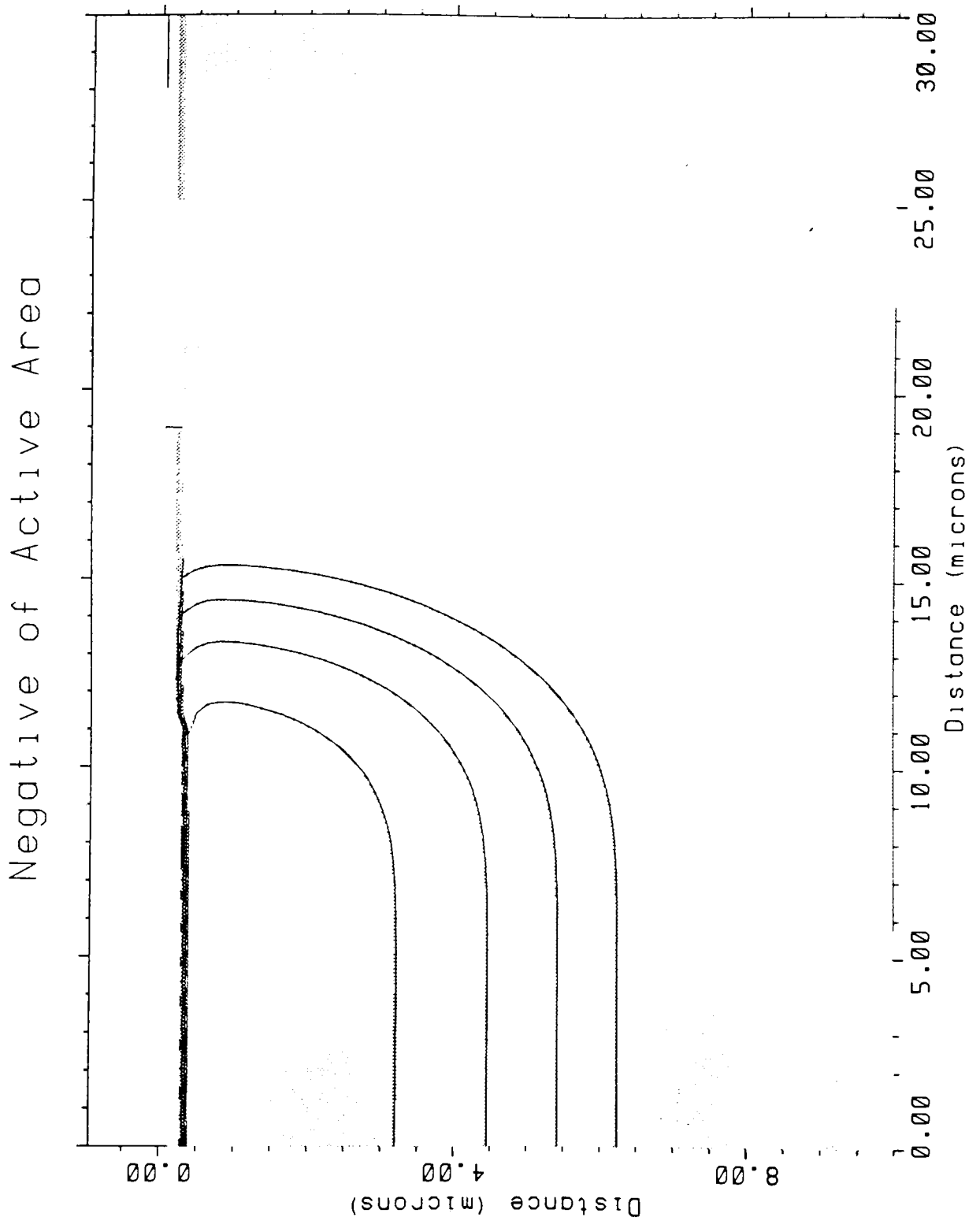
Cross section of well drive-in, boron contours from 1e14 to 1e16

Fig 4.3



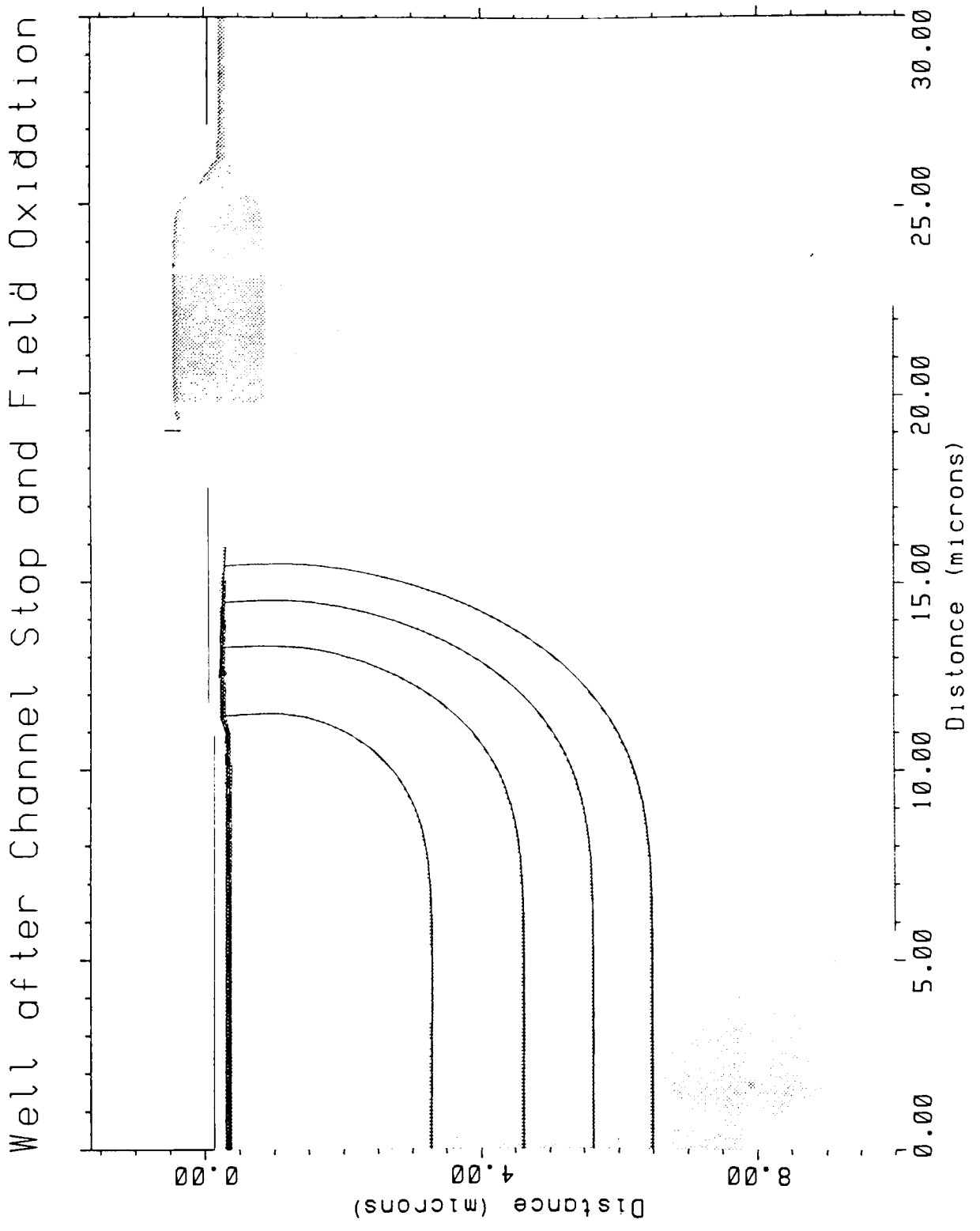
Cross section of pad oxide and nitride deposition

Fig 4.4



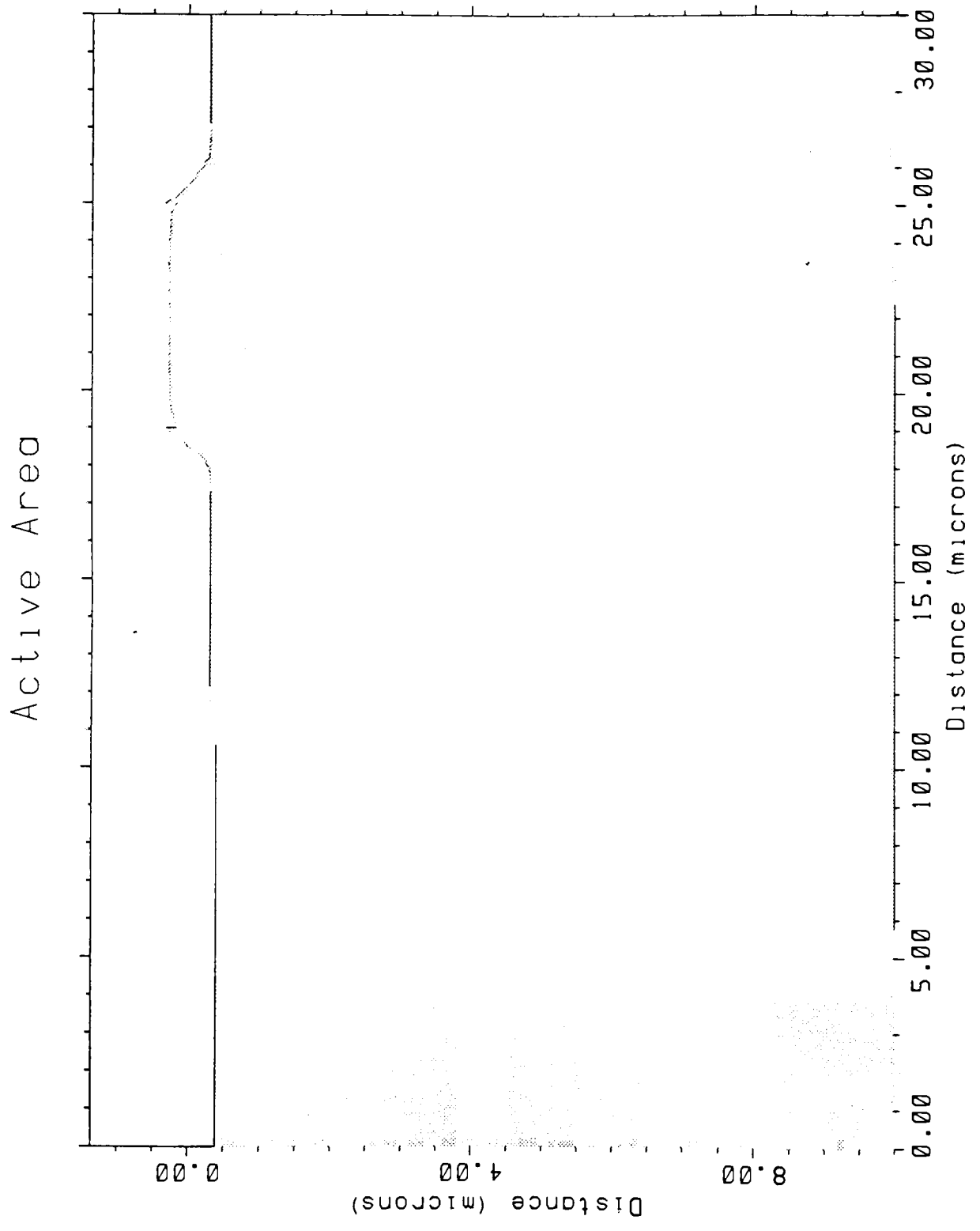
Cross section of negative of active area

Fig 4.5



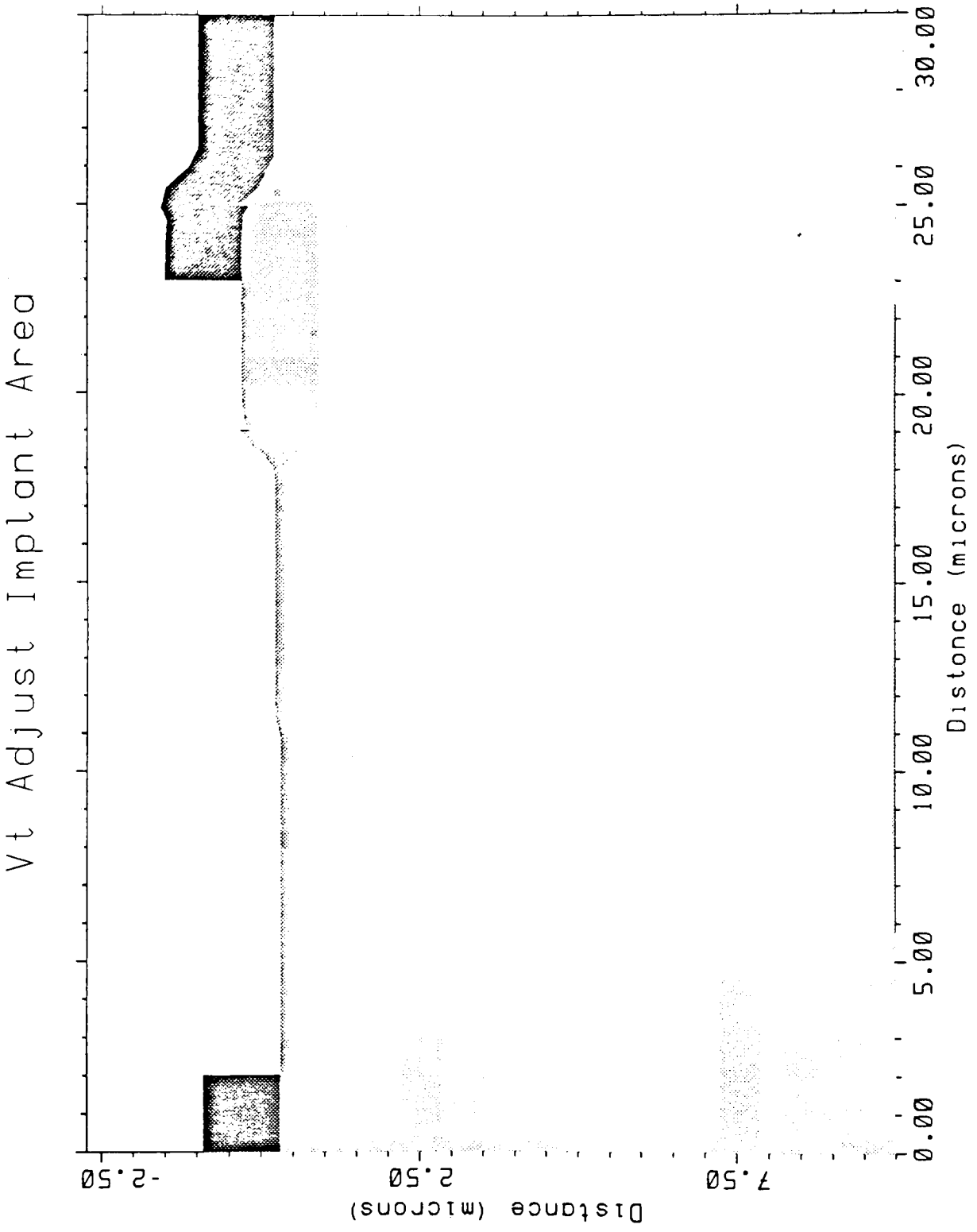
Cross section of well after channel stop and field oxidation

Fig 4.6



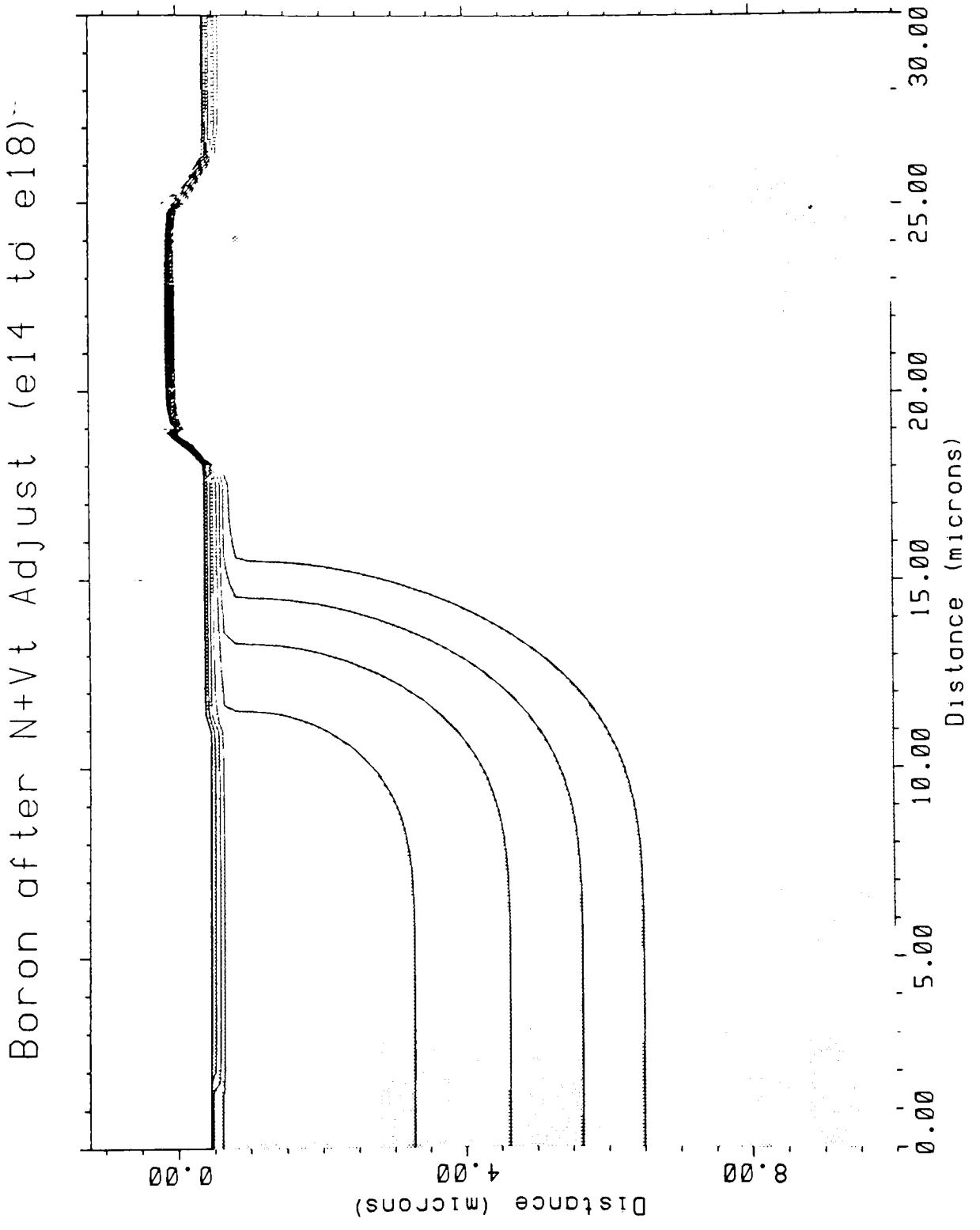
Cross section of active area

Fig 4.7



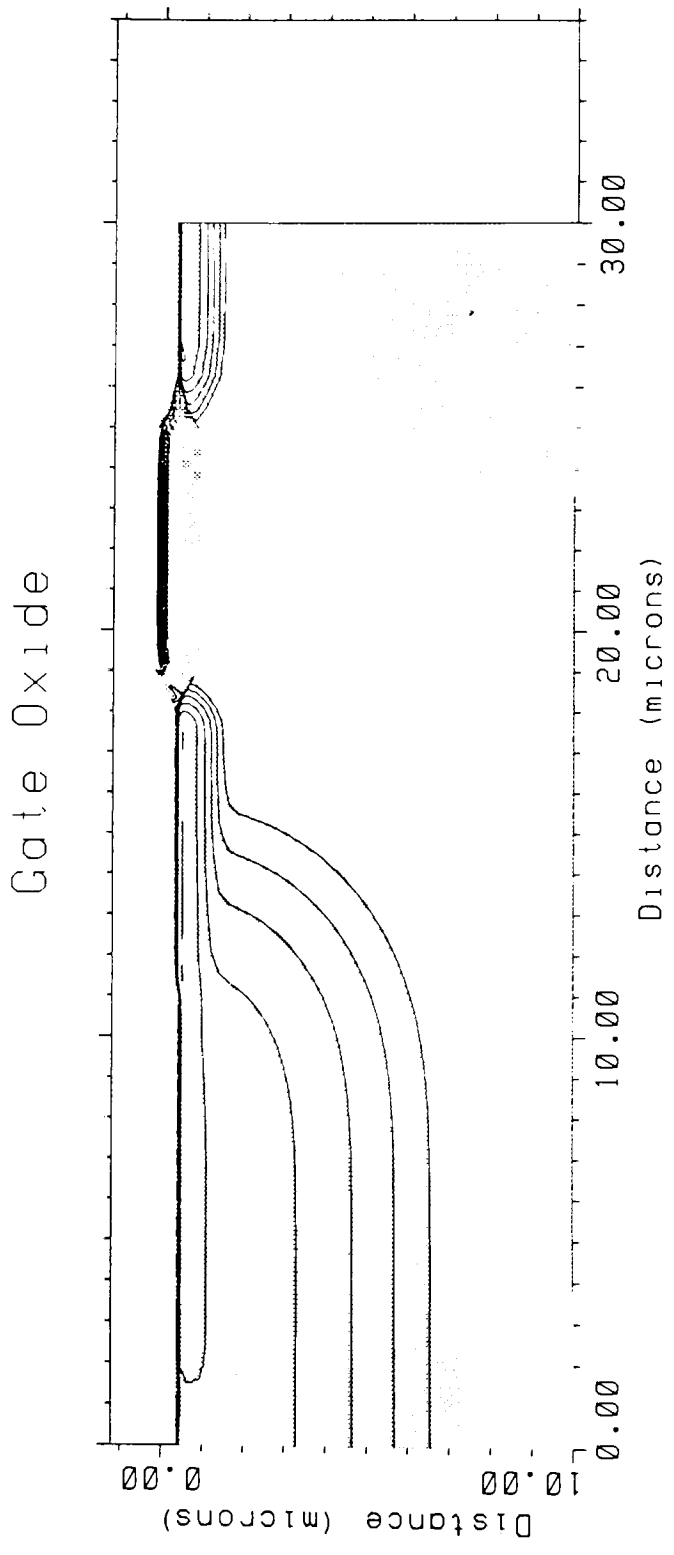
Cross section of Vt adjust implant area

Fig 4.8



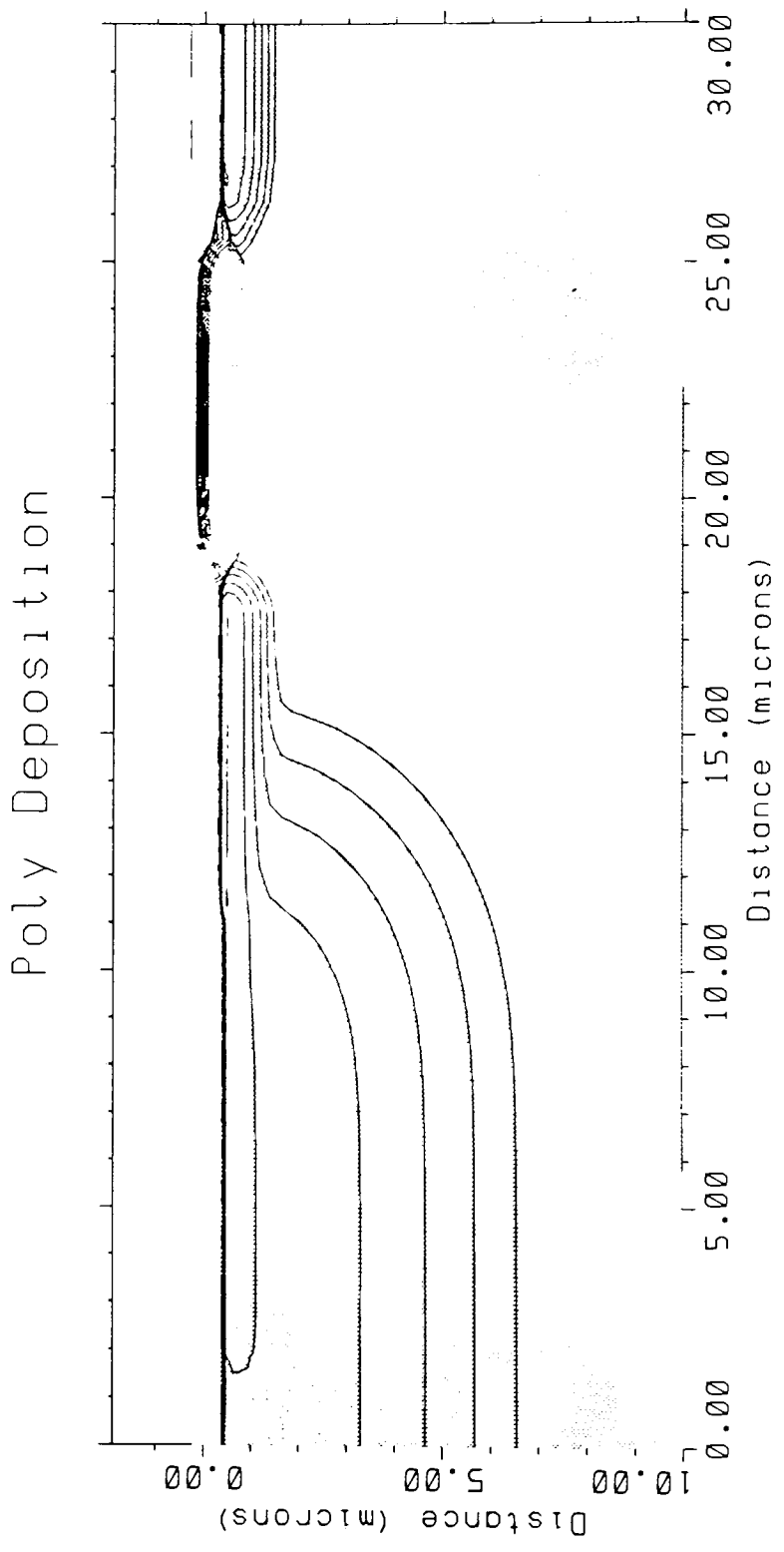
Cross section of boron concentration after N+ Vt adjust, (1e14 to 1e18)

Fig 4.9



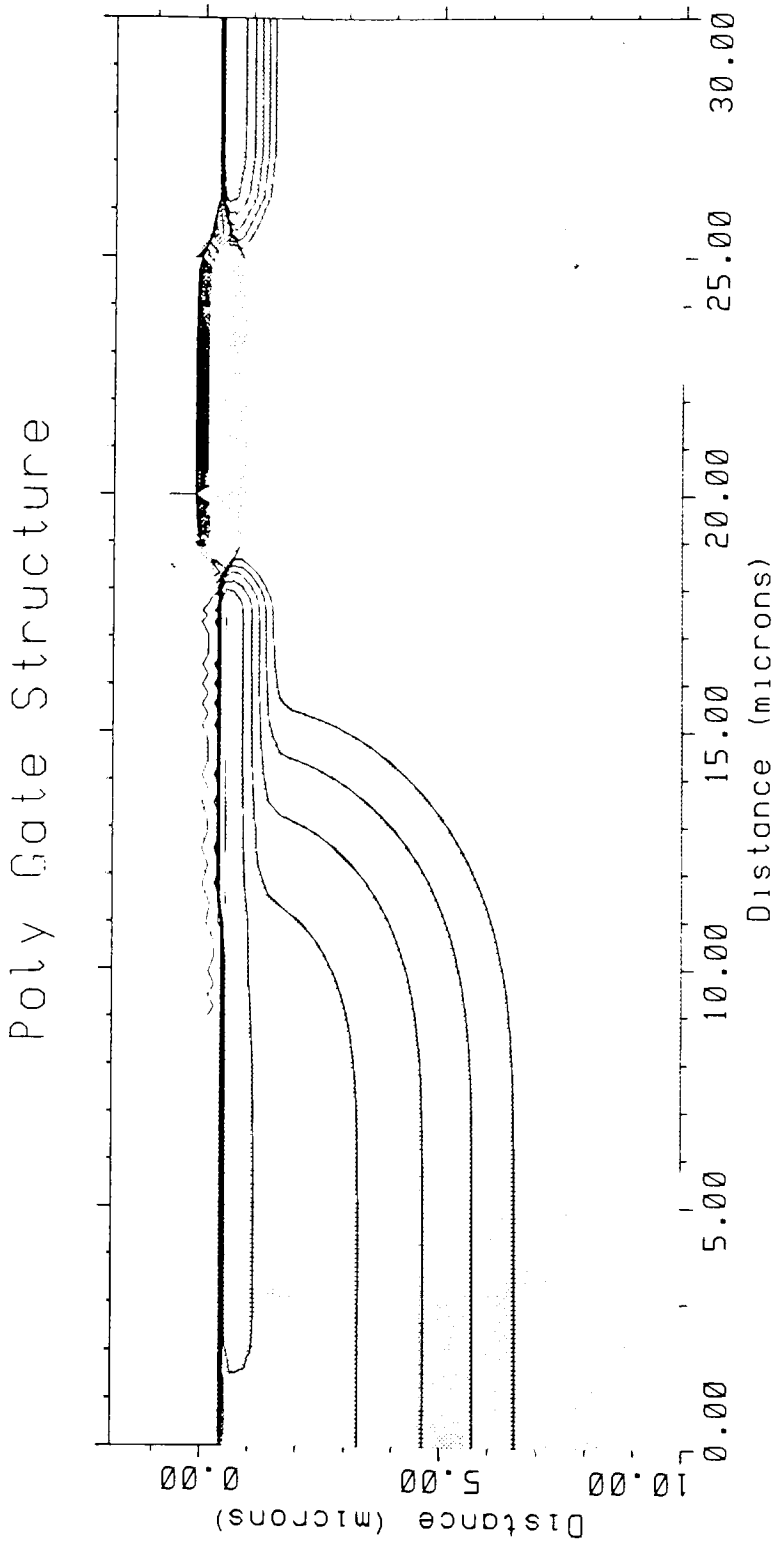
Cross section of gate oxide

Fig 4.10



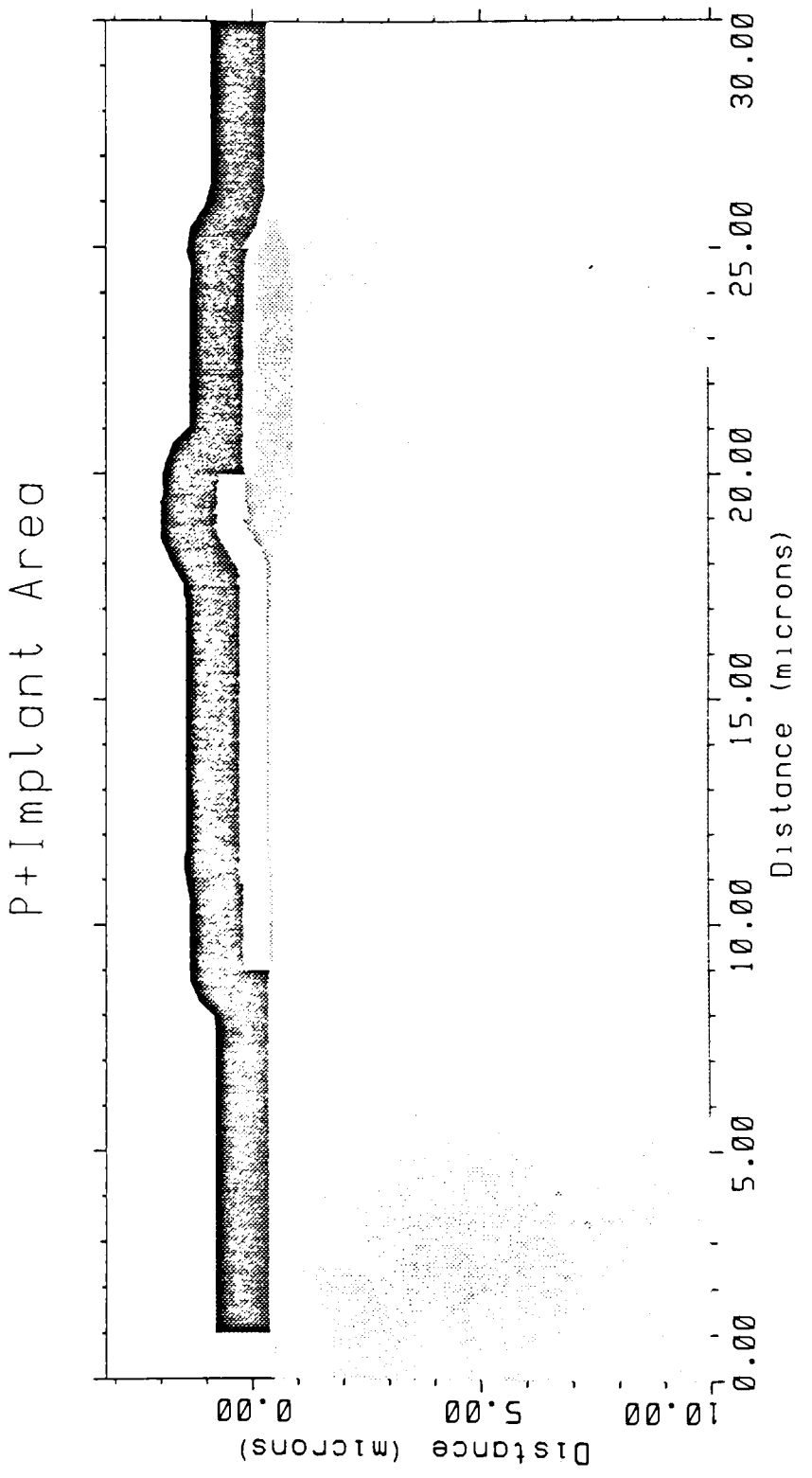
Cross section of poly deposition

Fig 4.11



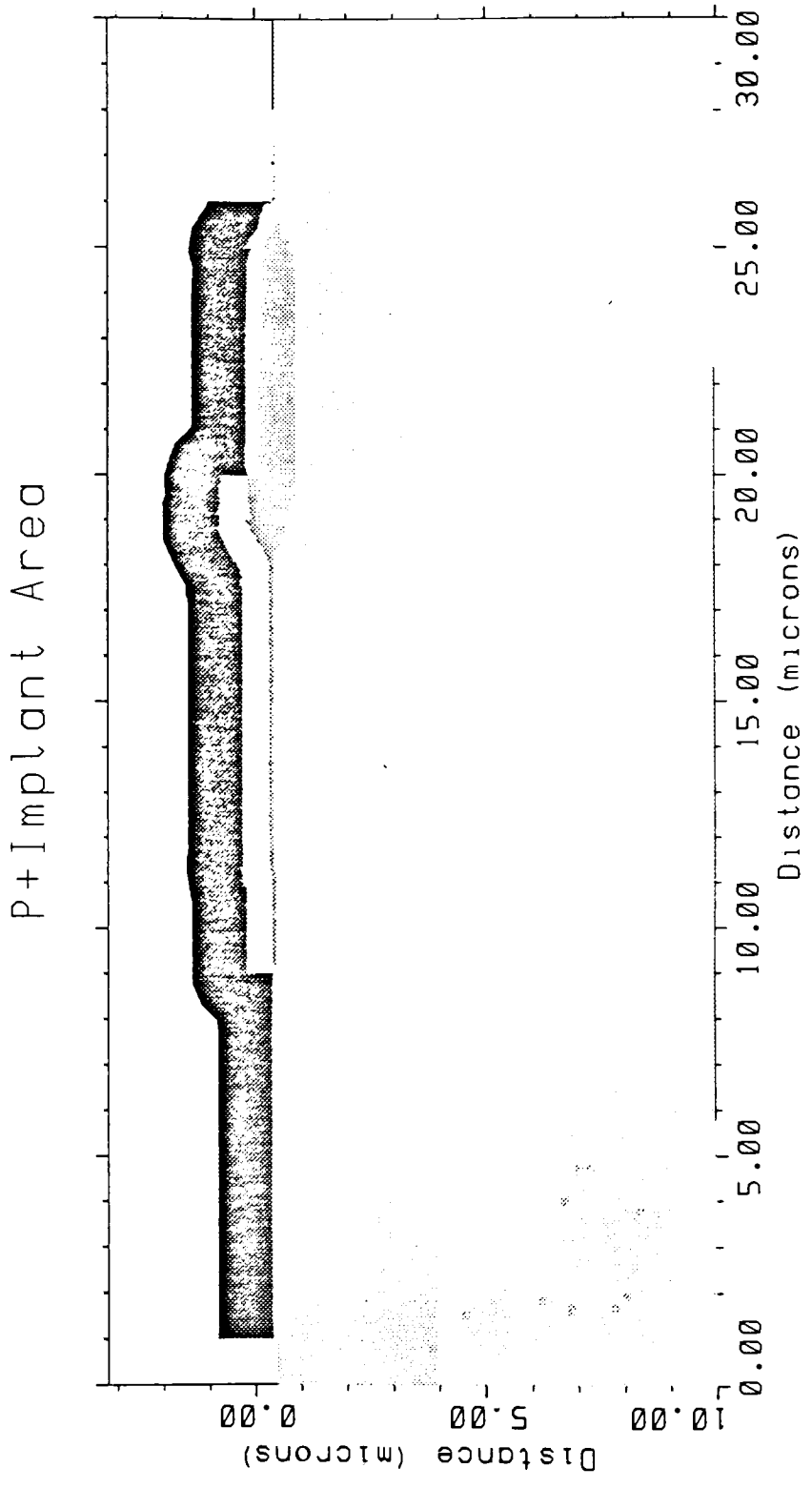
Cross section of poly gate structure

Fig 4.12



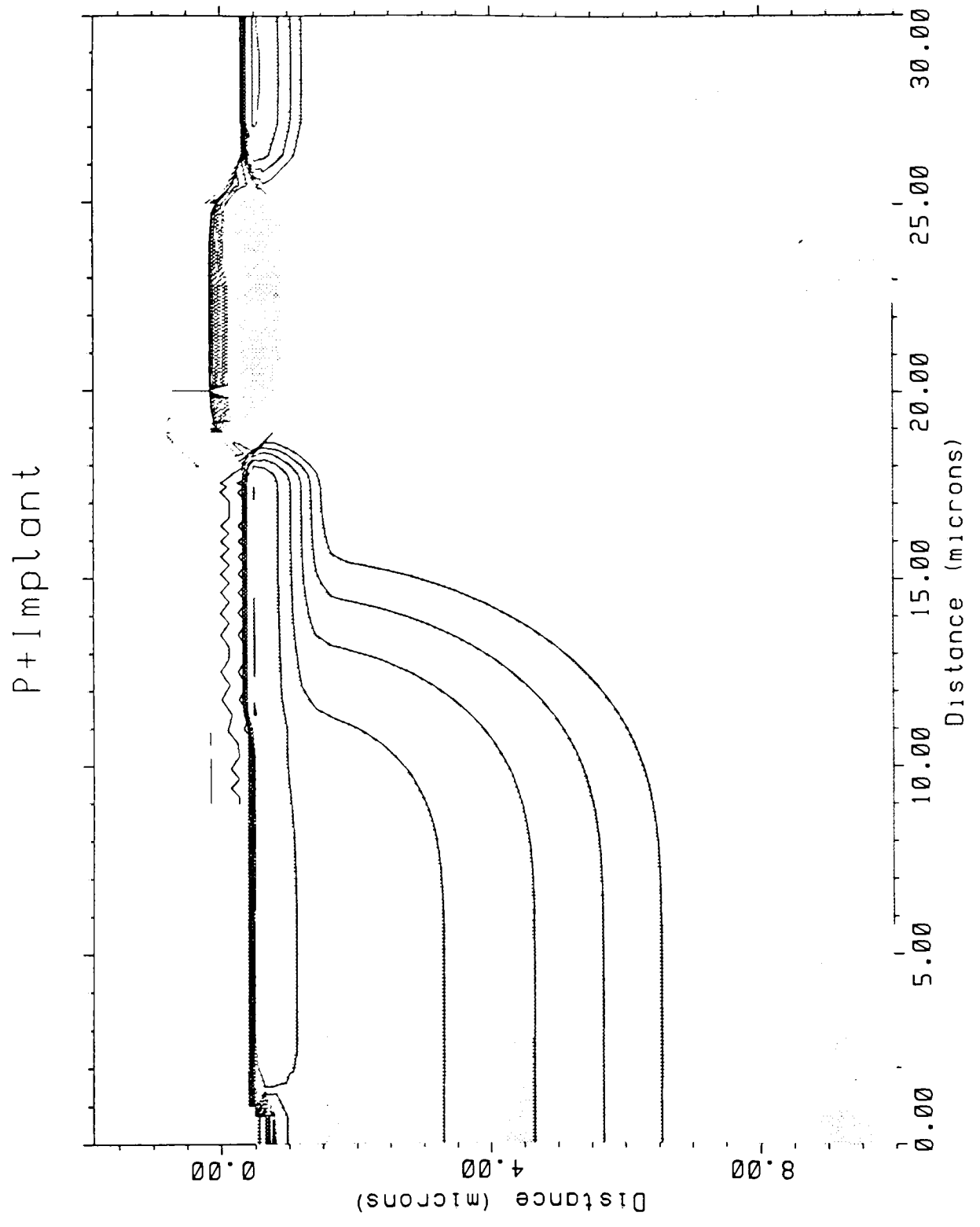
Cross section of P+ implant area for MOSFET

Fig 4.13



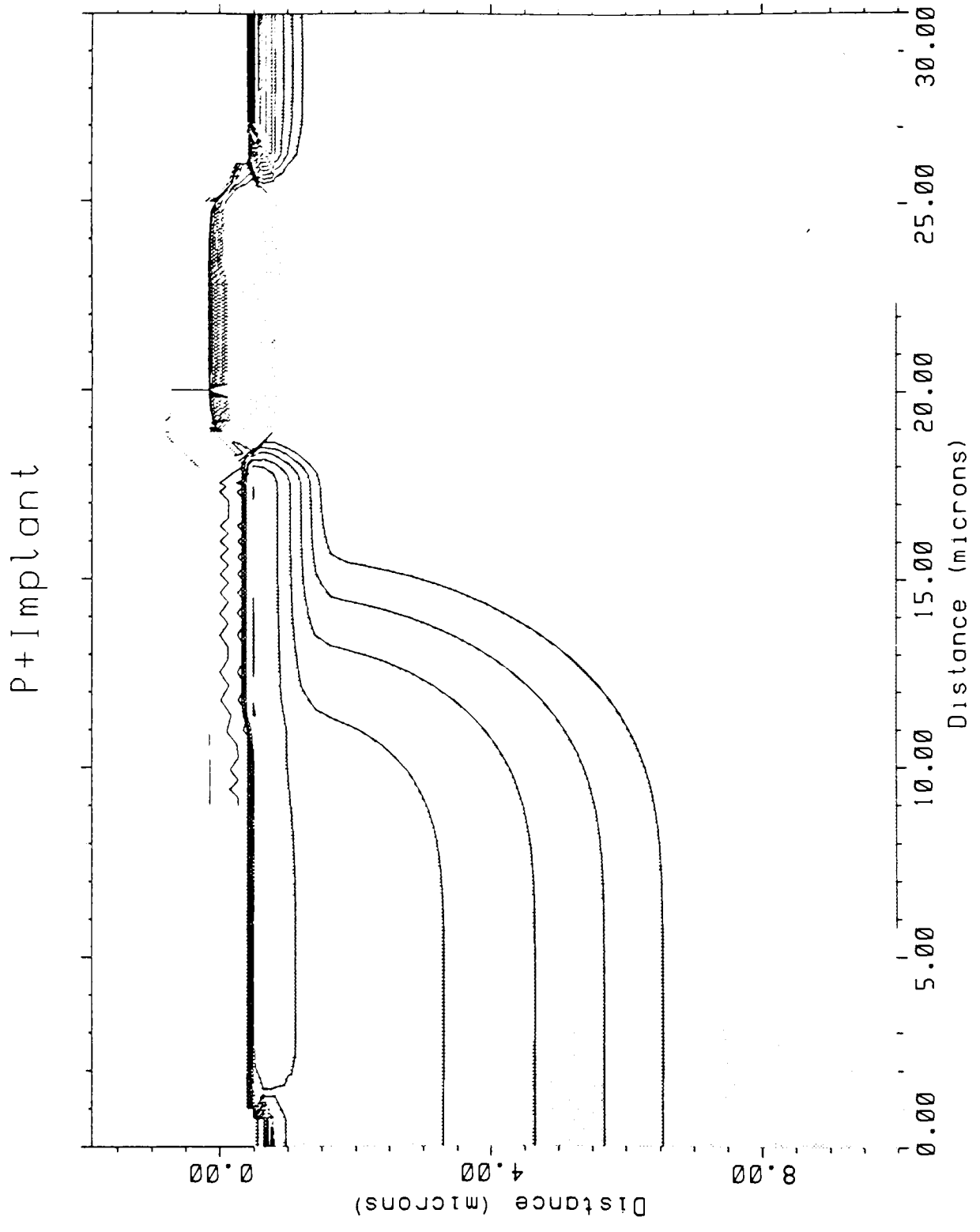
Cross section of P+ implant area for IGBT

Fig 4.14



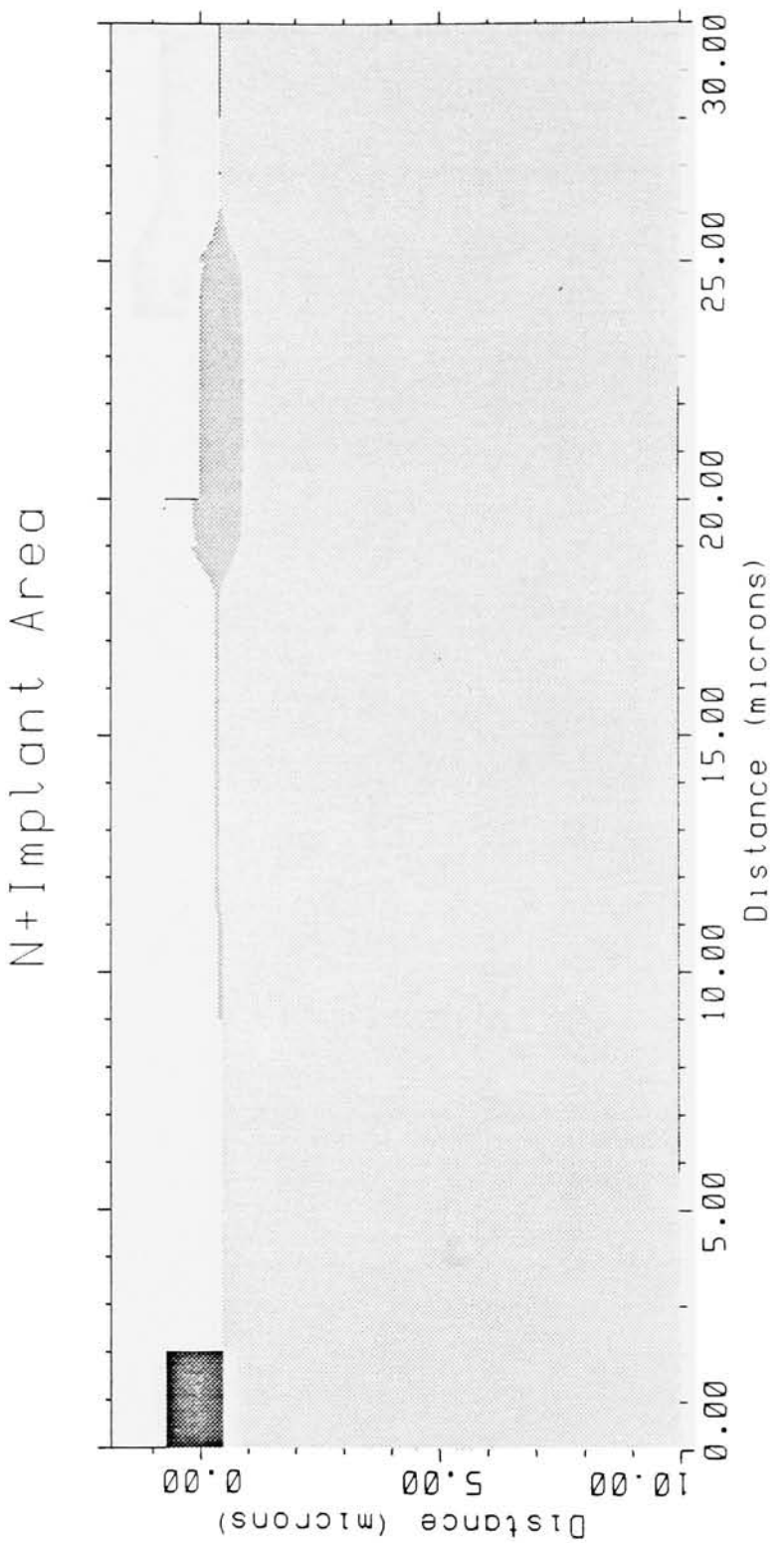
Cross section of P+ implant showing concentration, (1e14 to 1e20), MOSFET

Fig 4.15



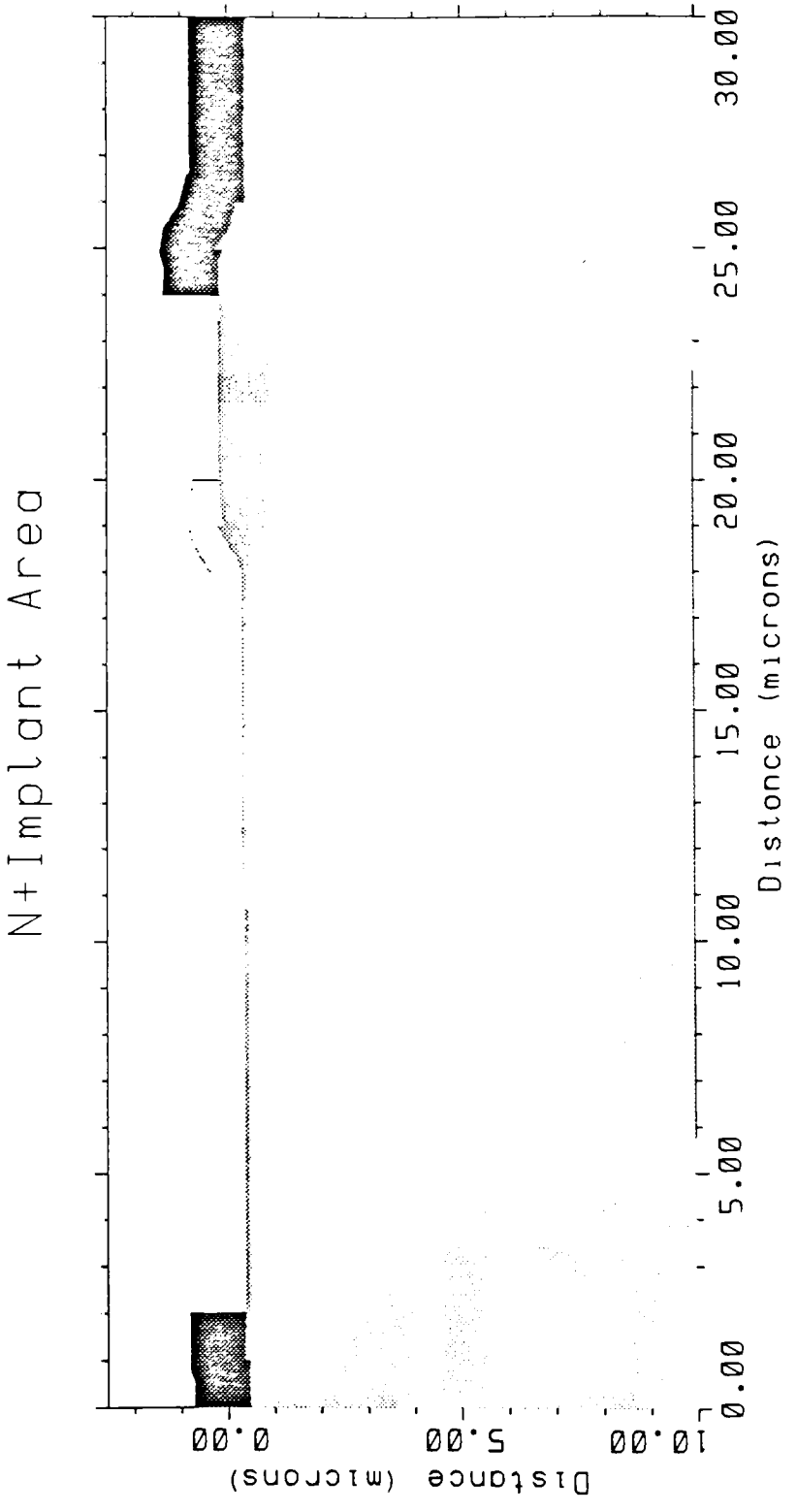
Cross section of P+ implant showing concentration, (1e14 to 1e20), IGBT

Fig 4.16



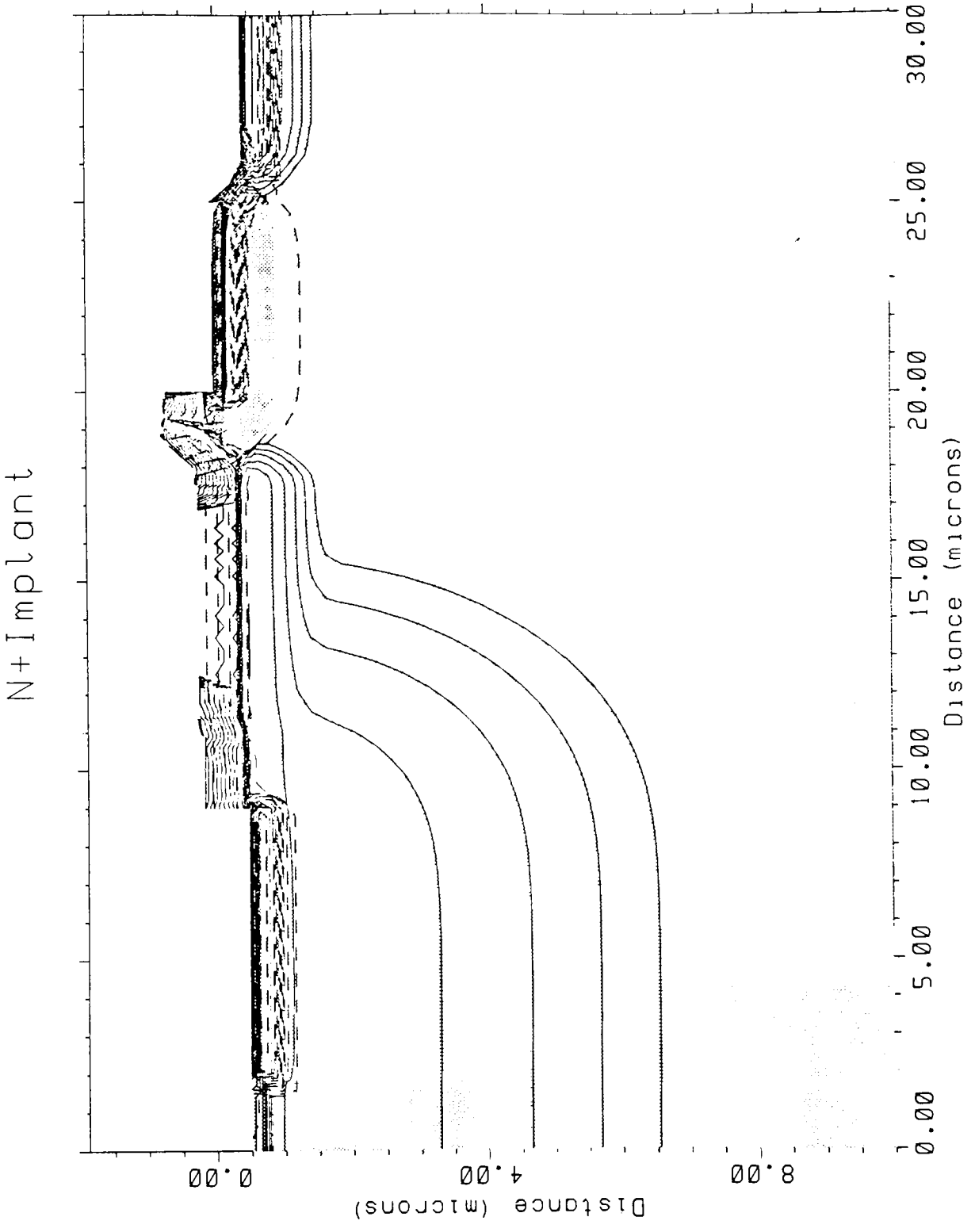
Cross section of N+ implant area, MOSFET

Fig 4.17



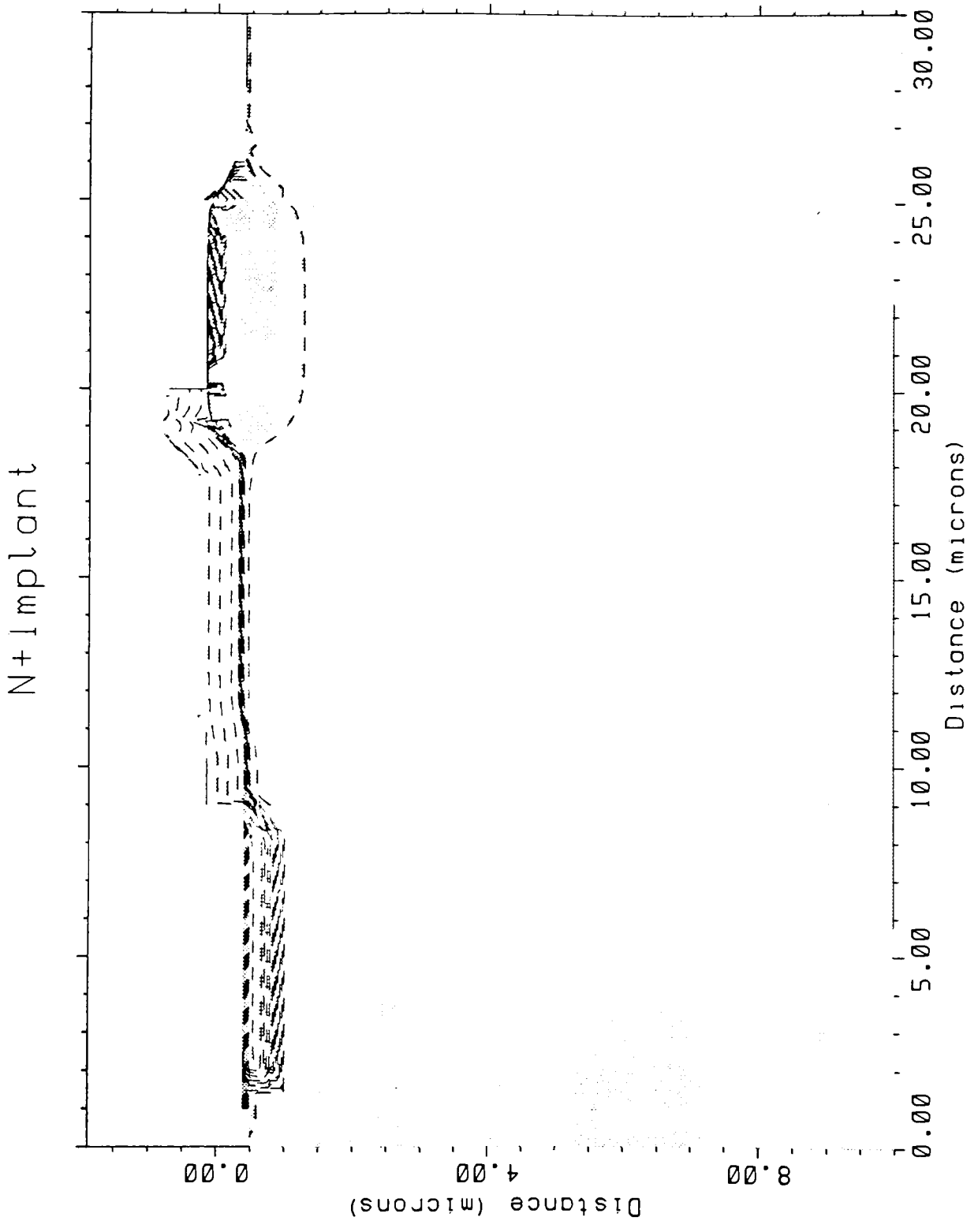
Cross section of N+ implant area, IGBT

Fig 4.18



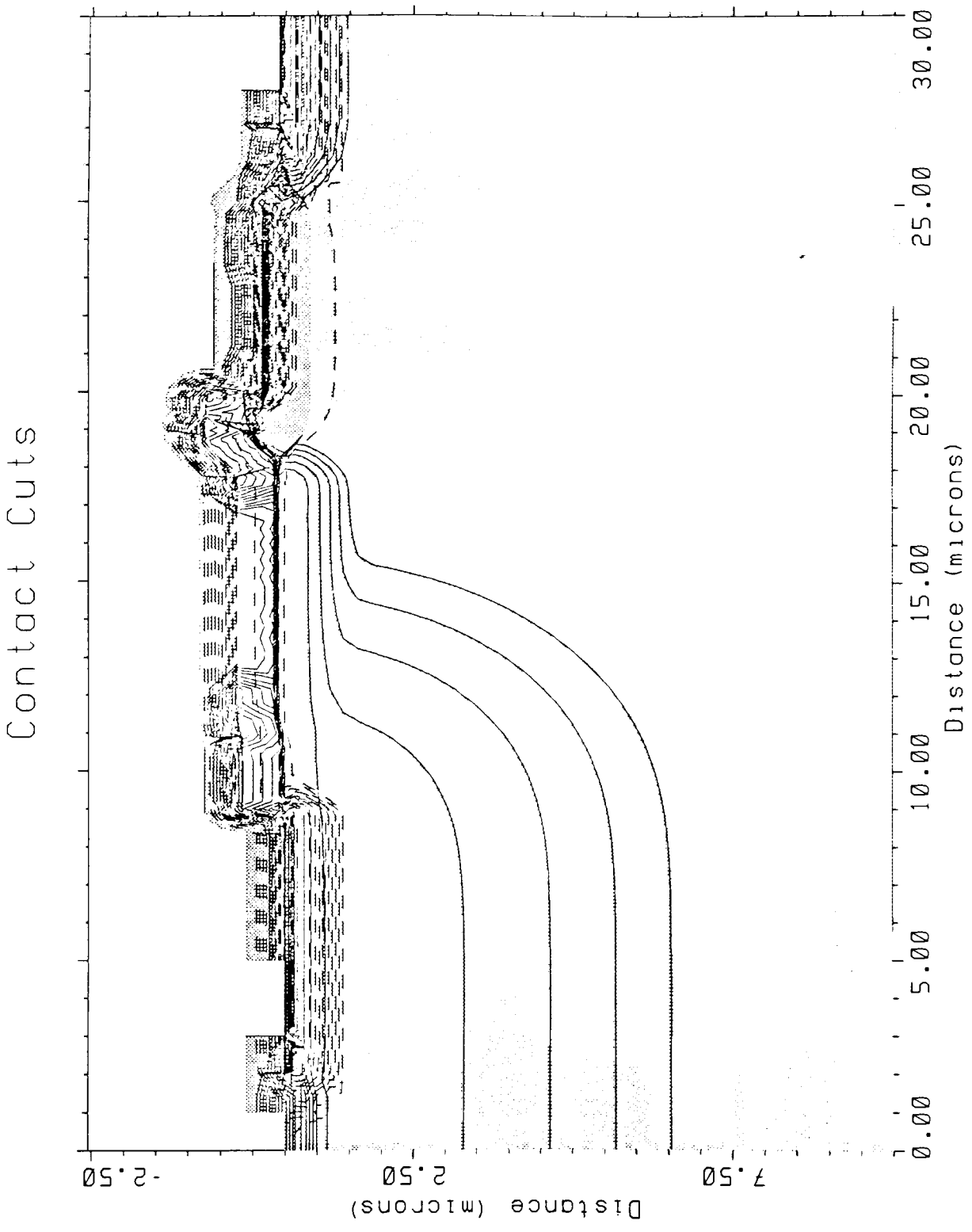
Cross section of N+ implant concentration, (1e14 to 1e18), MOSFET

Fig 4.19



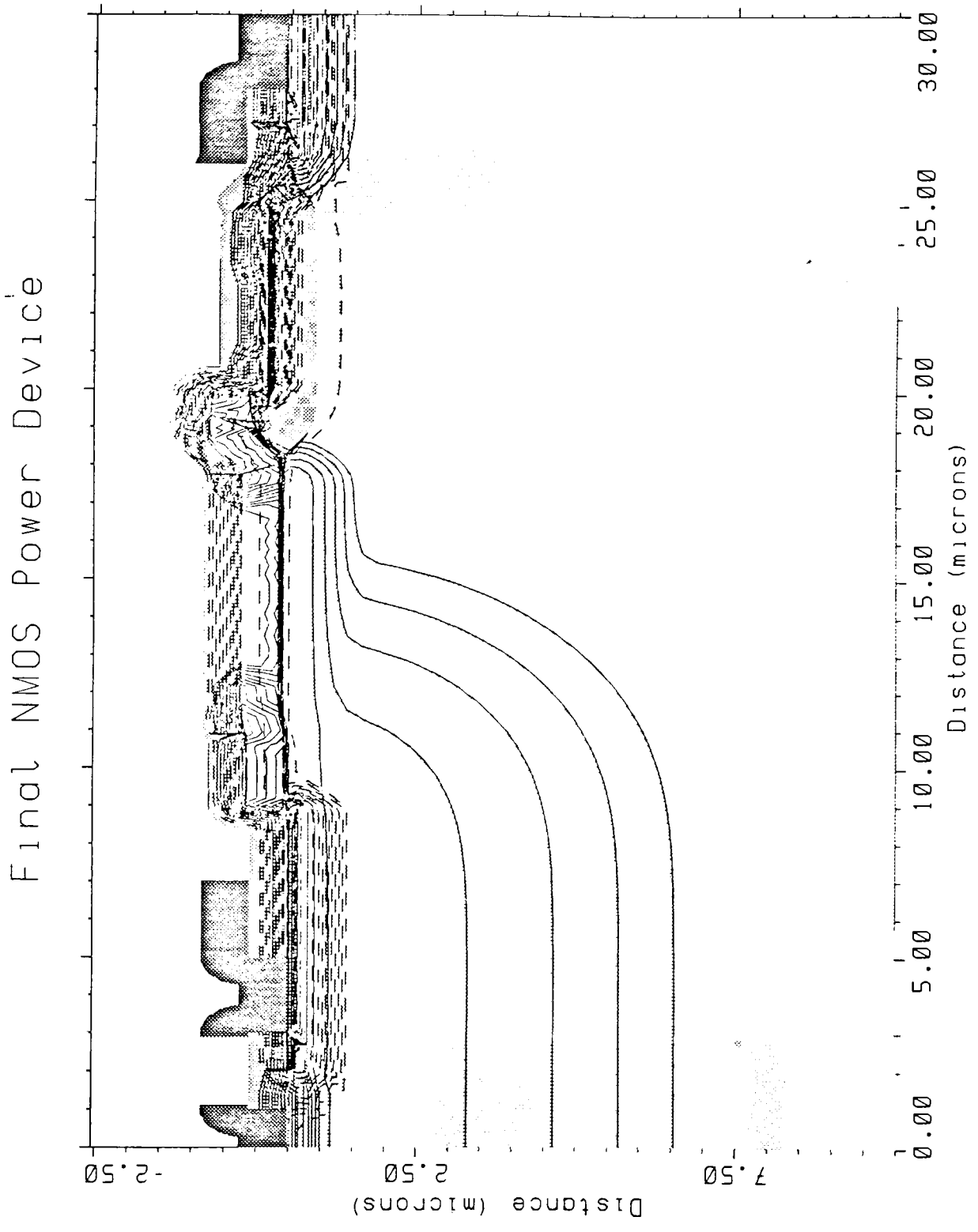
Cross section of N+ implant concentration, (1e14 to 1e18), IGBT

Fig 4.20



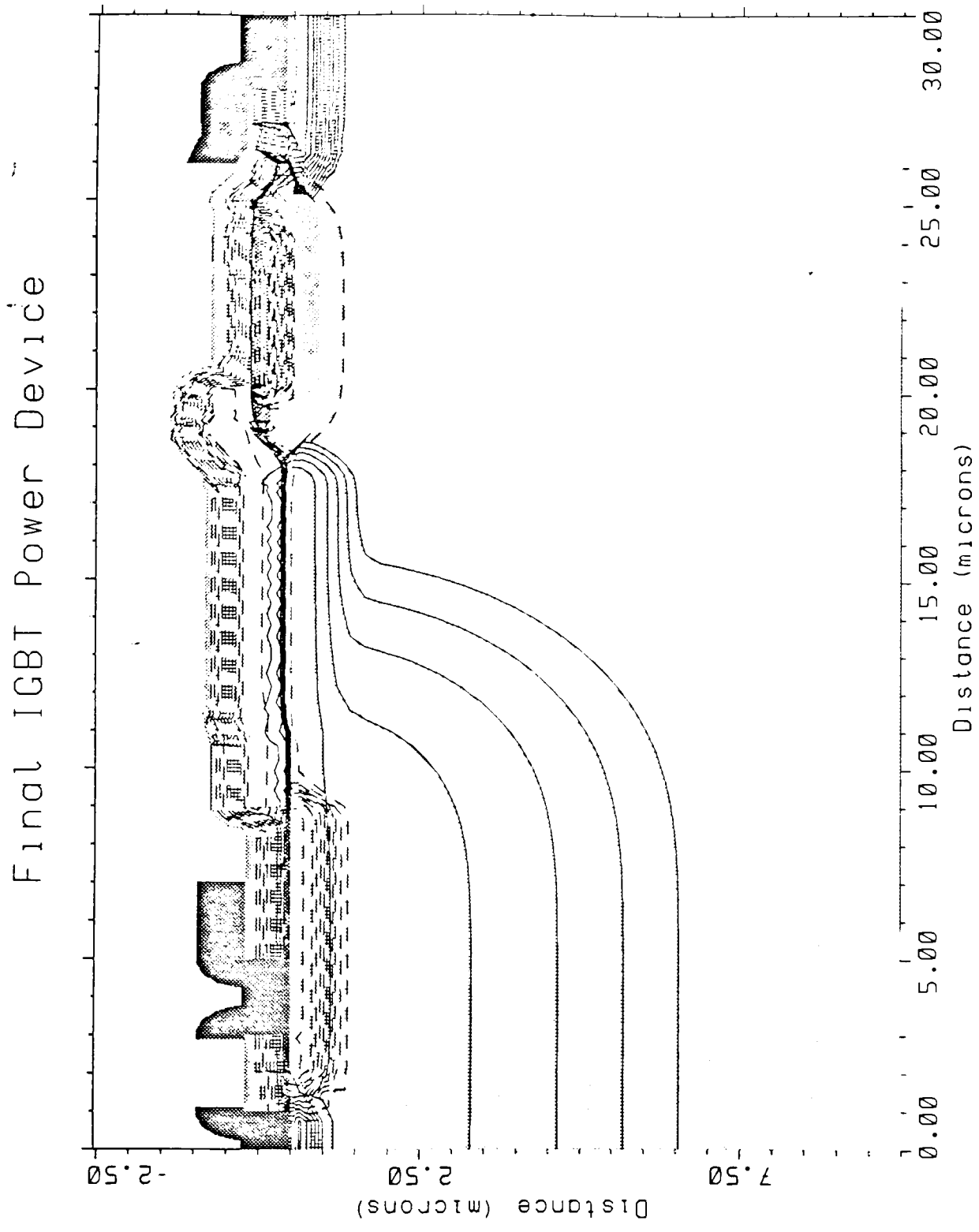
Cross section of contact cuts for both devices

Fig 4.21



Cross section of final NMOSFET device showing concentration contours

Fig 4.22



Cross section of final IGBT device showing concentration contours

Fig 4.23

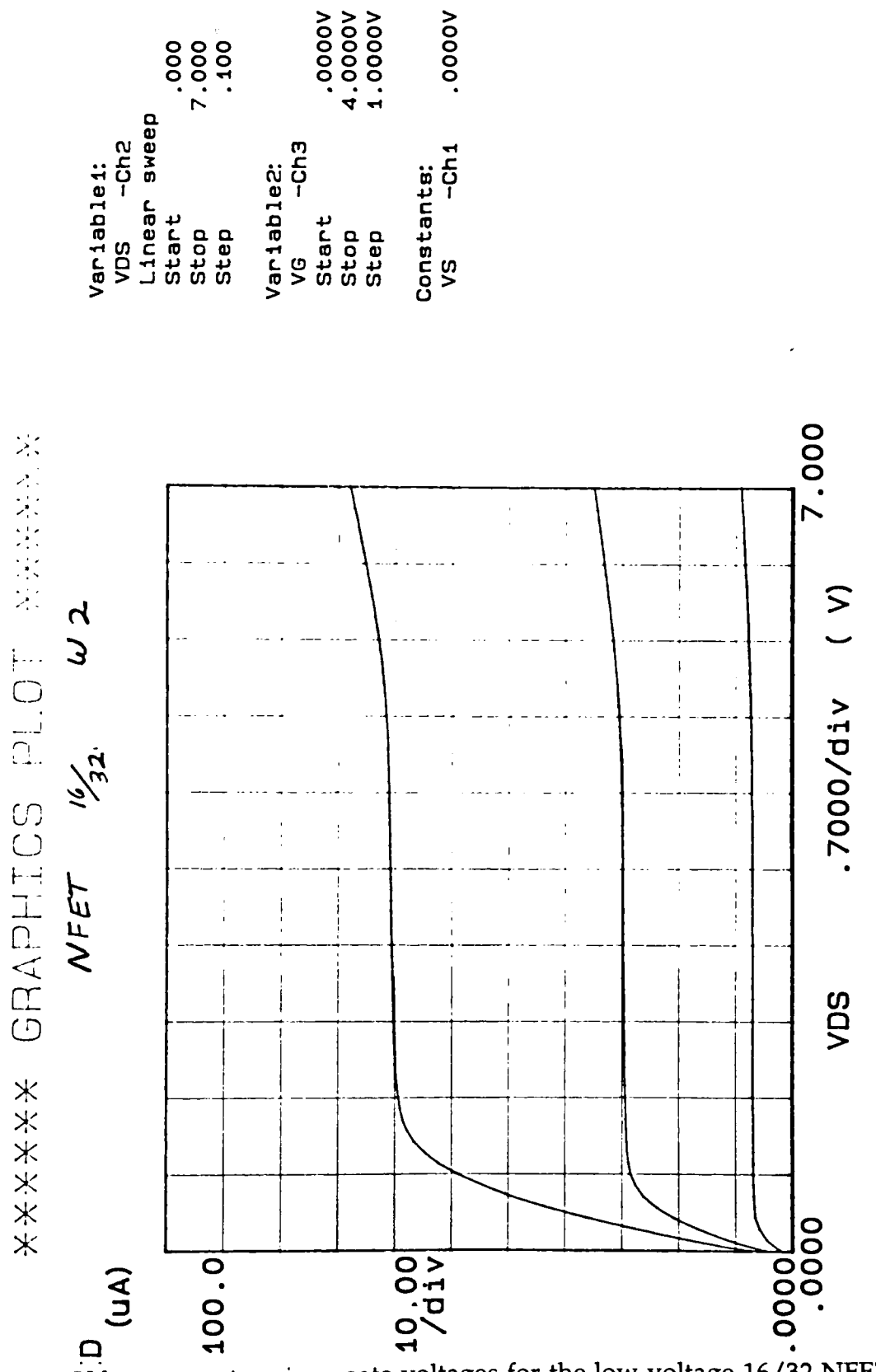
5. Electrical Testing

All wafers were tested on the HP4145 Parameter Analyzer. Both the power devices and the CMOS test structures were evaluated. The NMOS devices on the CMOS test chip were investigated but the PMOS devices were not due to a mask problem. The original design of the P-well CMOS test chip utilized both a P and an N well. When the mask was made, the two wells were made one. Therefore, the PMOS devices are made in a P-well and act like resistors not transistors. The low voltage NMOS devices were used as a preliminary guide to asses the functionality of the chips. With the operation of the CMOS portion of the wafers confirmed, the power devices were tested. The power devices were evaluated on maximum operating current, on-state resistance and voltage blocking capability. The power devices were initially tested with the use of the parameter analyzer to determine which dies were functionally acceptable. The devices that passed the initial screening were further evaluated on the Tektronix 370 Programmable Curve Trace. This instrument is a more appropriate piece of equipment for the power device testing than the HP4145 because its voltage and current ratings are larger than those of the HP4145 which is limited to 100V and 100mA.

By confirming the operation of the low voltage devices it can be concluded that the CMOS process was successful. Any problems that are encounter regarding the power device indicate changes to the design and process of the power device alone.

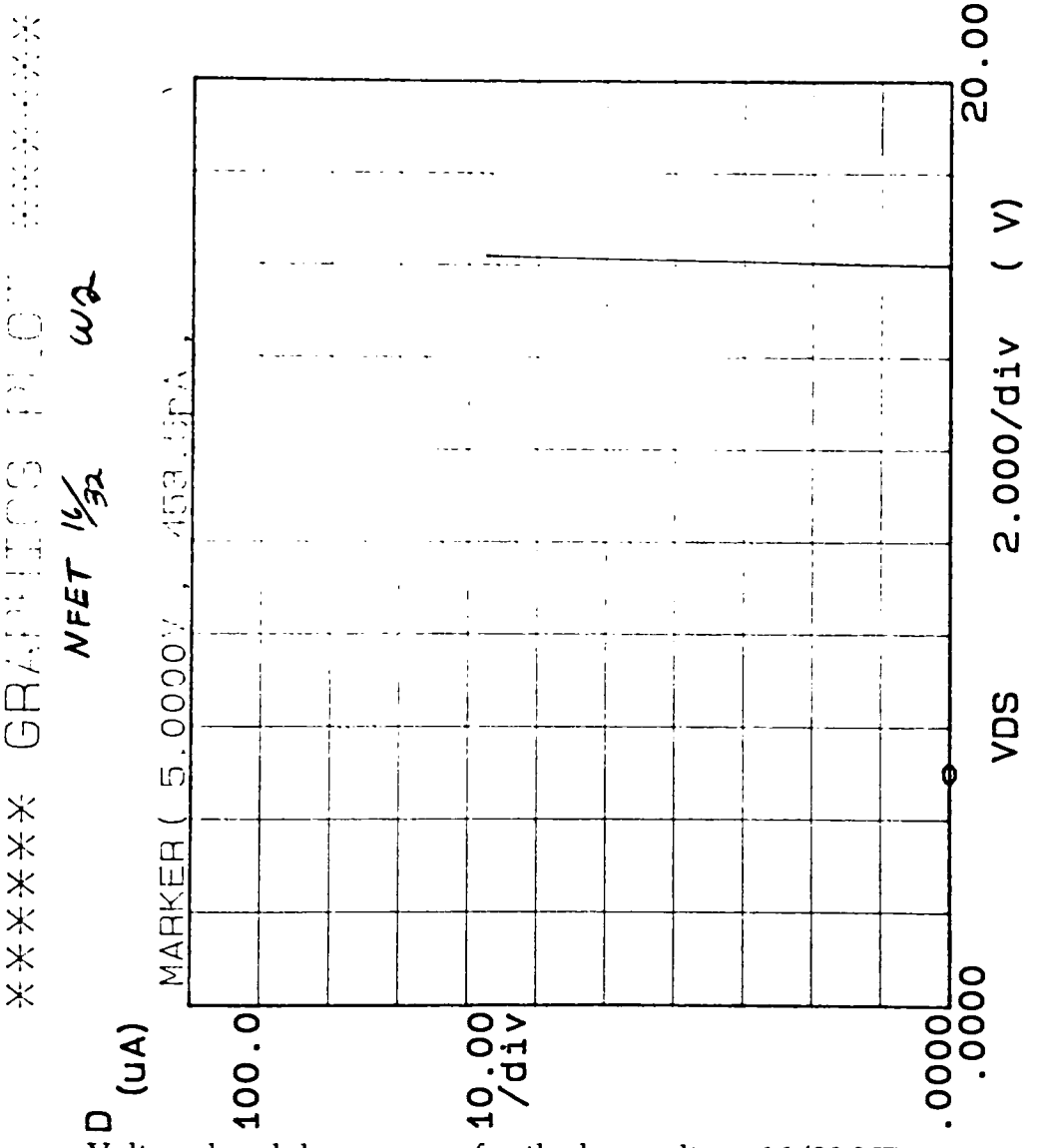
Fig 5.1 and Fig 5.2 show the Ids vs. Vds characteristics for the on-state and off-state output of the low voltage 16/32 NMOS structure on the CMOS test chip. Numerous tests were performed at various sights on the wafers and these figures are typical for this device type. Other NMOS test structures of different channel width and length values were also tested and results were similar. Other test structures, such as resistors and field oxide transistors were also tested to extract more parametric information regarding the process.

From Fig 5.1 and 5.2 the on-state resistance, the operating current, the threshold voltage and the breakdown voltage can be determined. The on-state resistance of the device is Ω. For this device, the saturation Ids value for a Vgs of 4V is 70 μA. (Fig 5.1). The threshold voltage is approximately 2v. (Fig 5.1) Finally, the source to drain breakdown voltage of the low voltage NMOS transistor for a Vgs of 0V is about 16v. (Fig 5.2) These points will be used to make comparisons with the ratings of the power devices.



Ids vs Vds curves at various gate voltages for the low voltage 16/32 NFET

Fig 5.1

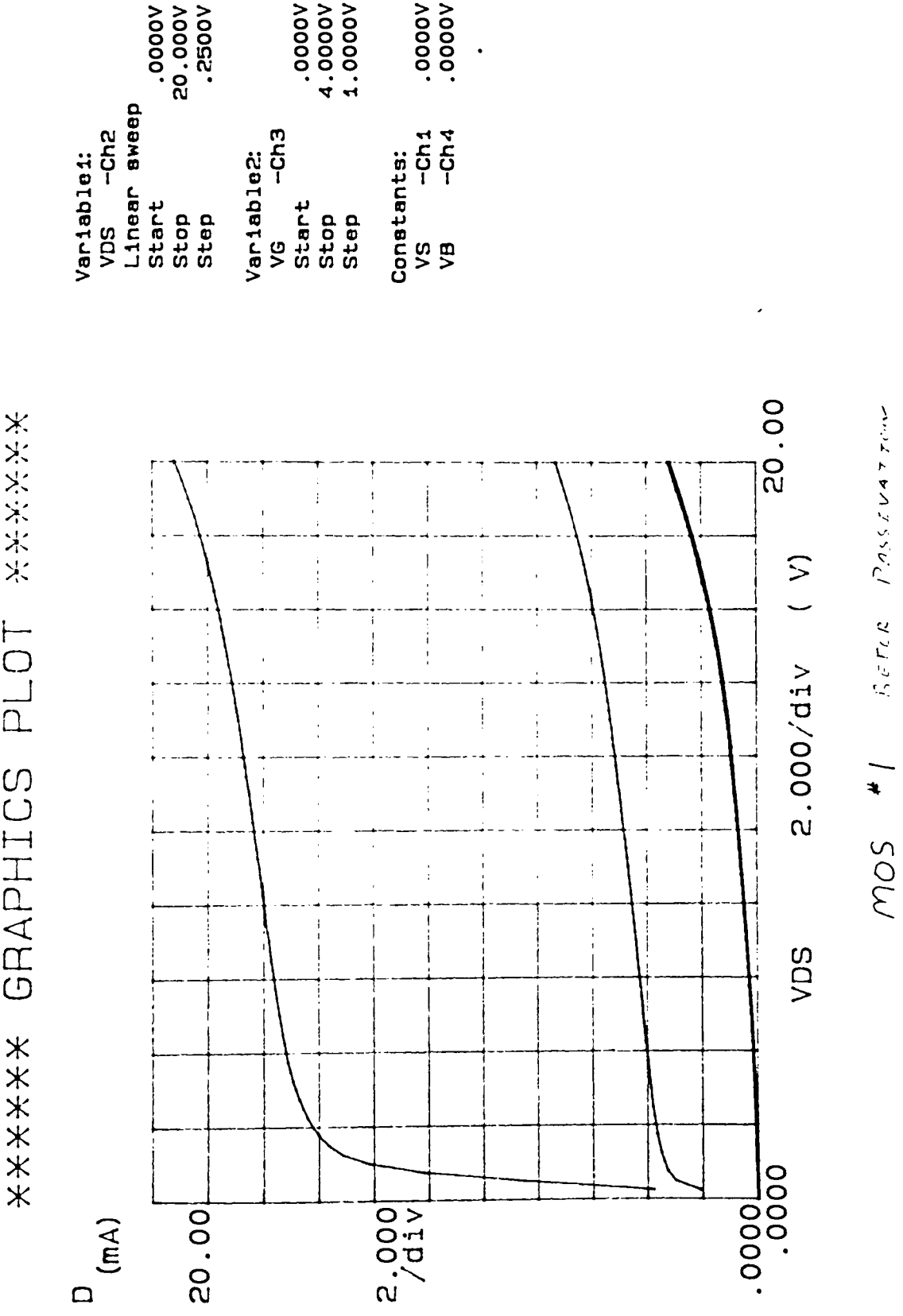


Voltage breakdown curve for the low voltage 16/32 NFET

Fig 5.2

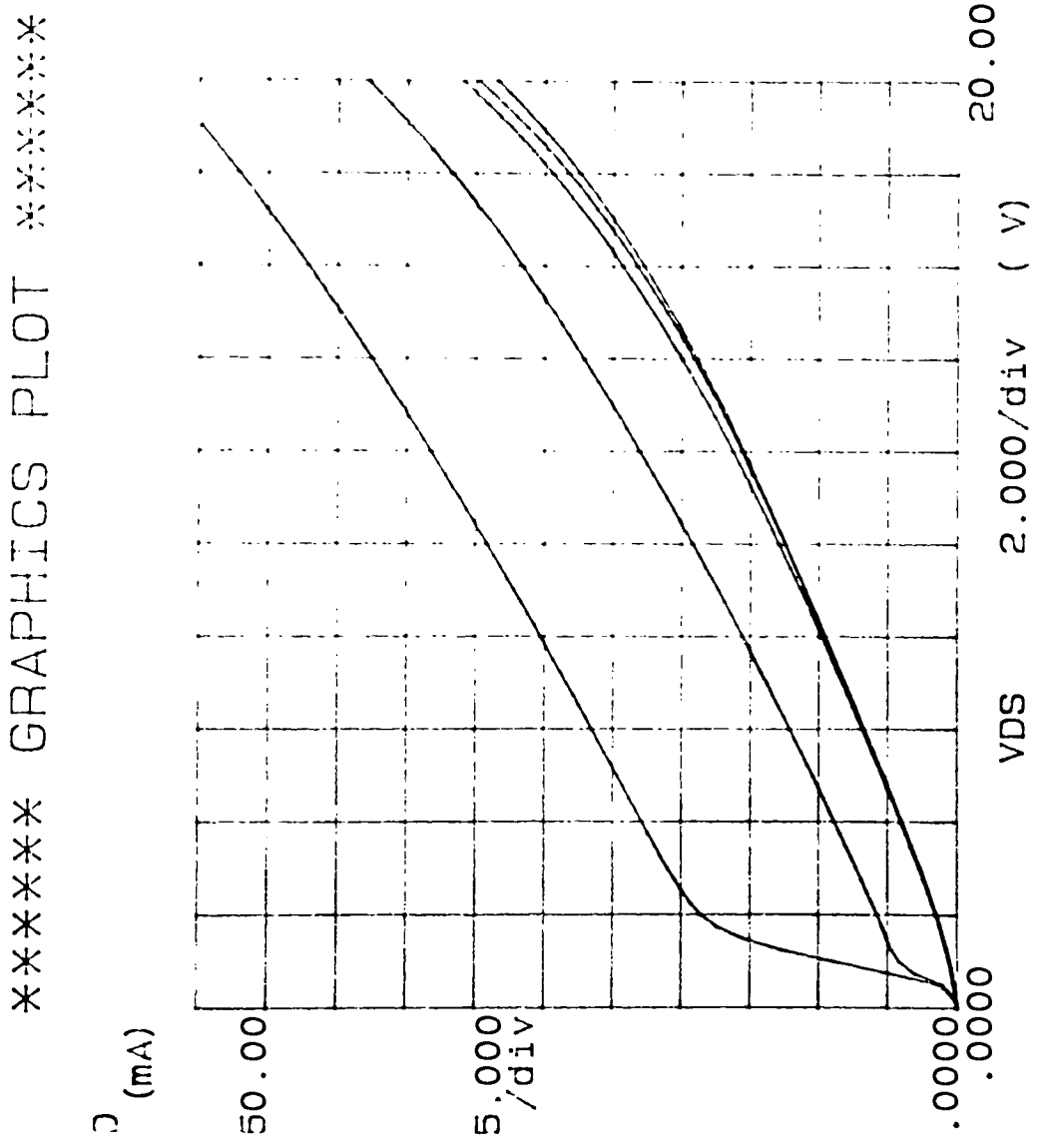
The power devices were tested initially on a HP4145. Fig 5.3 and Fig 5.4 show the output Ids vs. Vds curves for the Power MOS and IGBT respectively. Contrary to theoretical predictions the IGBT curve shows more on-state resistance than expected. This problem was traced to a mask error. The field for the P+ implant was reversed and consequently the drain did not receive the P+ implant. This indicates that the metal contact at the drain is to the lightly doped N substrate. The IGBT is not studied further because of the lack of the P+ drain region.

The tests revealed a severe leakage problem for all power devices. Fig 5.5 is an expanded view of Fig 5.3 and shows the extent of the leakage problem more clearly. The on-state current shows an increase of more than double the normal operating current due to the leakage problem. Devices operating at 16mA increased to the current limit of 40mA in 15V. It was from this finding that we decided to add a passivation layer and a via mask level. Fig 5.6 shows the same device after the passivation steps. The same device after the passivation layer showed a current increase, over the same voltage period, of only 15mA. The on-state current increased from 16mA to 31mA. The change in leakage current is apparent. The effects of the passivation layer are more pronounced at larger voltages.



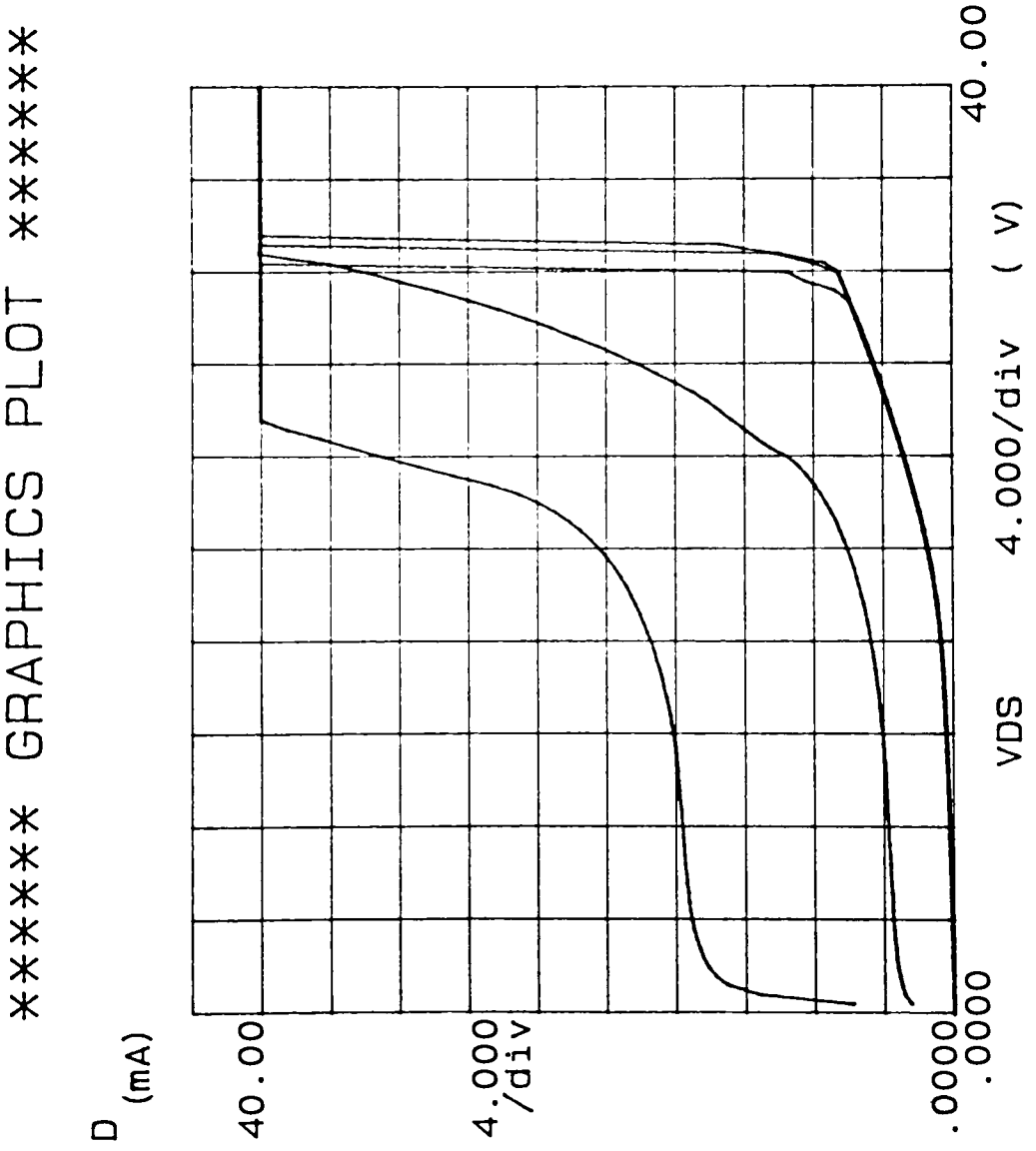
Ids vs Vds for the Power MOS #1 device without passivation layer

Fig 5.3



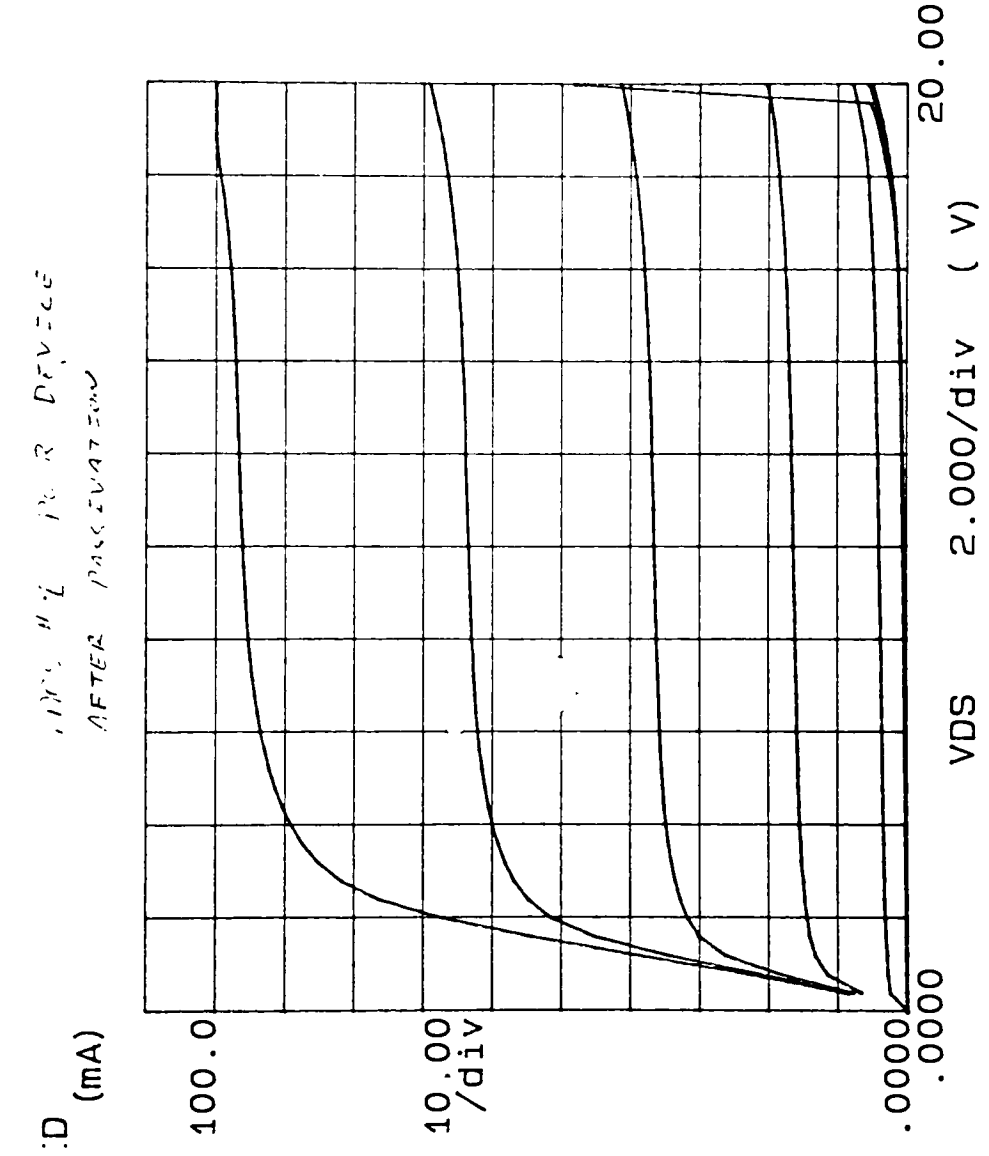
Ids vs Vds for the IGBT #1 device without passivation layer

Fig 5.4



Expanded view of Ids vs Vds for Power MOS #1 showing leakage

Fig 5.5

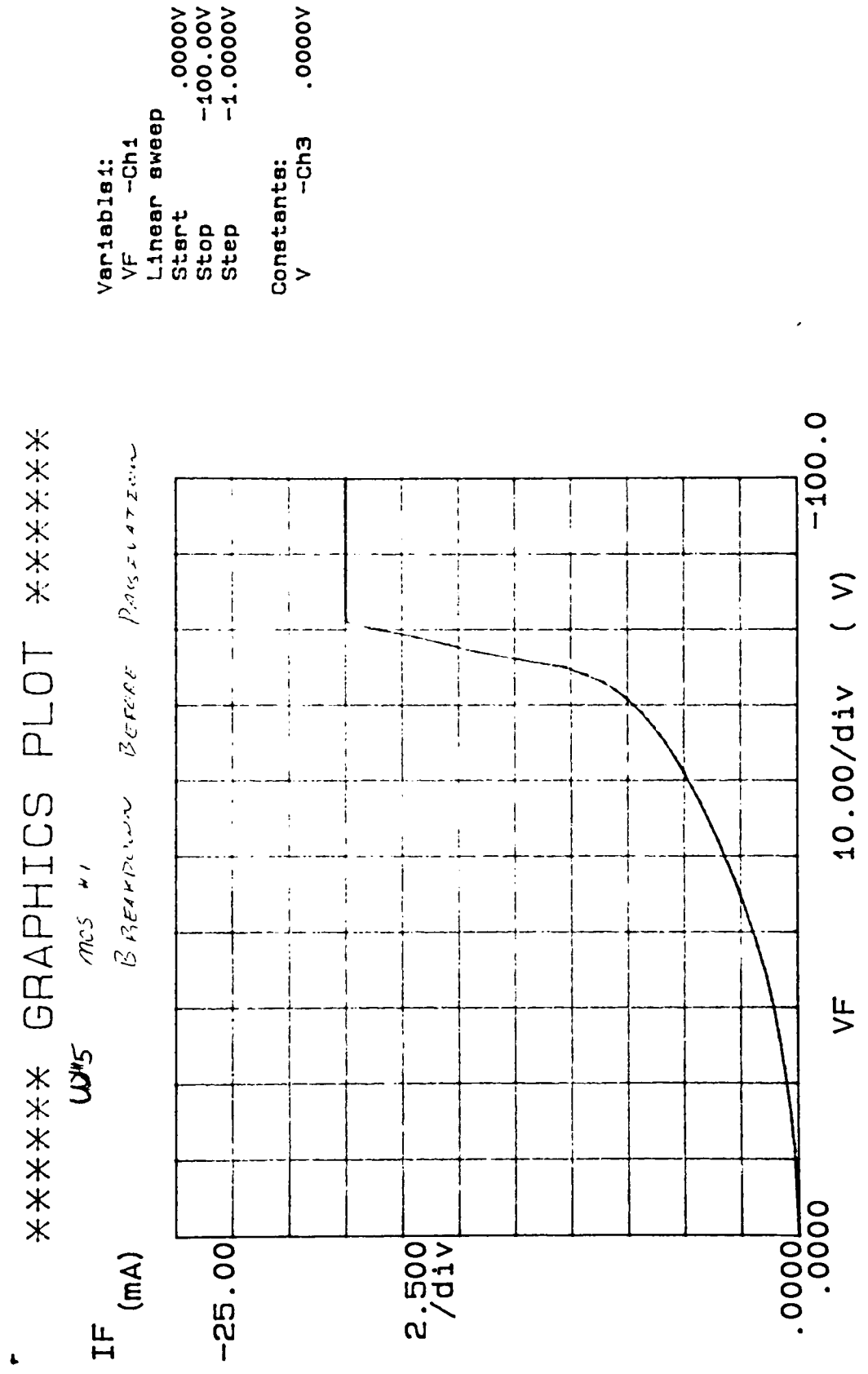


Ids vs Vds for the Power MOS #1 device with passivation layer

Fig 5.6

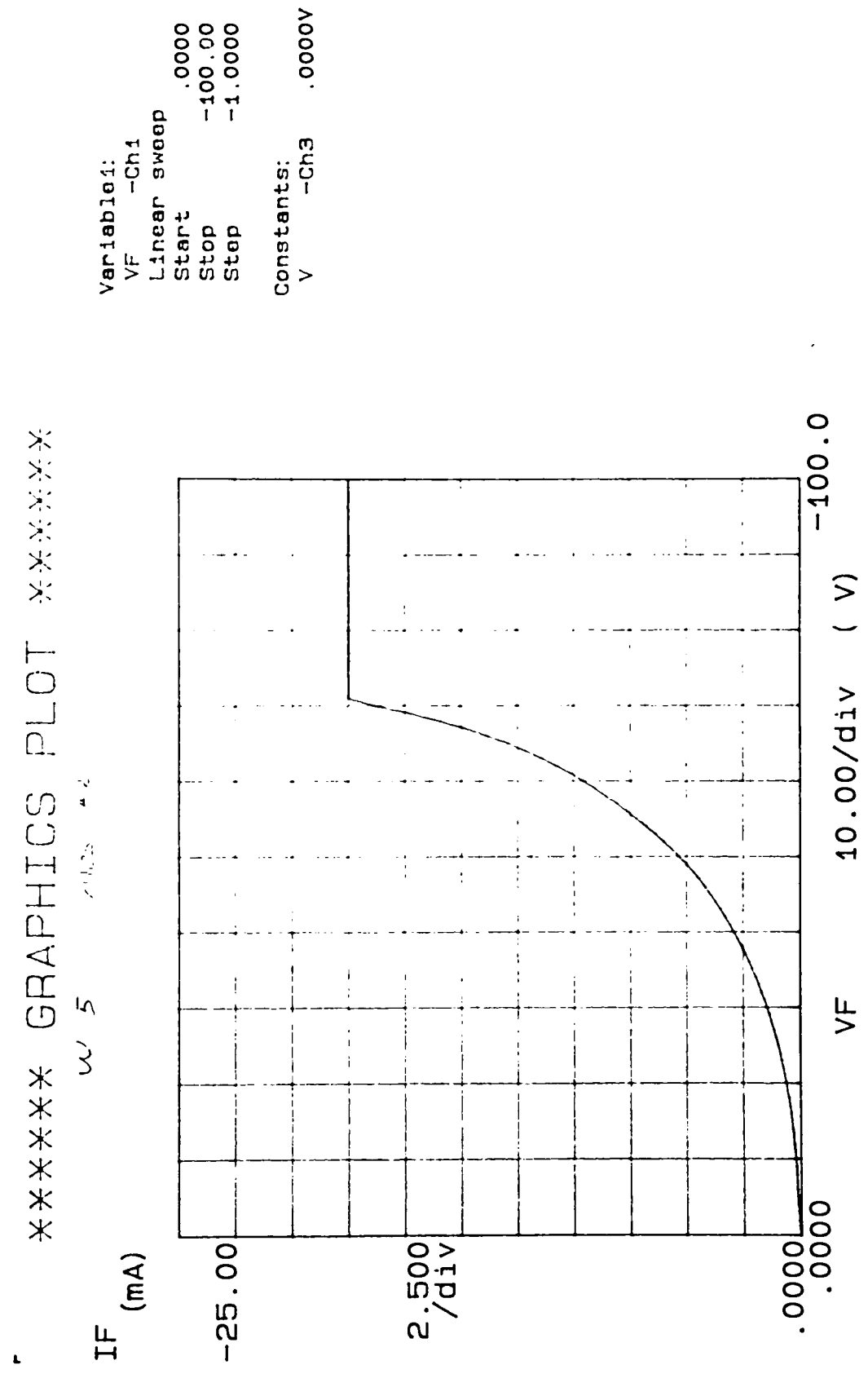
A breakdown voltage study was also performed before the device was tested on the Tektronics 370. Fig 5.7, Fig 5.8 and Fig 5.9 show the effects of the field plate overlap on the breakdown voltage. Fig 5.7 has the shortest gate length and the best breakdown voltage. As the gate length increases the breakdown voltage decreases. This is attributed to the increase in electric field due to potential crowding in the field oxide. With a smaller field oxide the electric field must increase. The breakdown was studied in the same manor as the low power devices. An actual breakdown curve is presented in Fig 5.10. This is presented to indicate the difference of leakage and breakdown. At 33 volts, the sharp increase in current is the breakdown point. The current indicated at 5.2v on the graph is much larger than in low power devices, but when compared to the 300mA of on-state operating current, a leakage of 155μA could be acceptable.

With the initial test performed and an idea of the characteristics, the devices were tested on the Tektronics 370 to determine the high power characteristics and limitations.



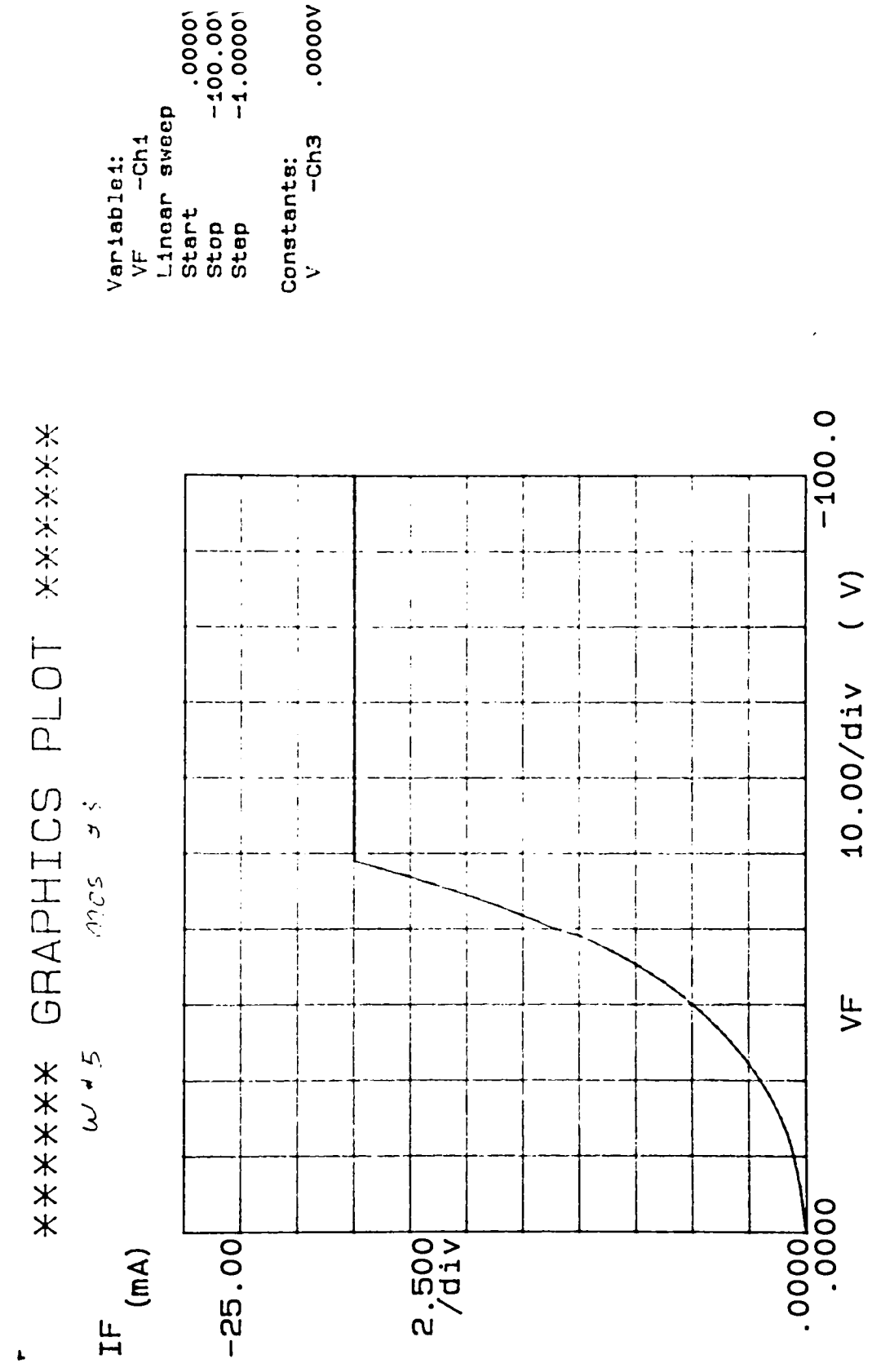
MOS #1, shortest field plate overlap, breakdown voltage without passivation

Fig 5.7



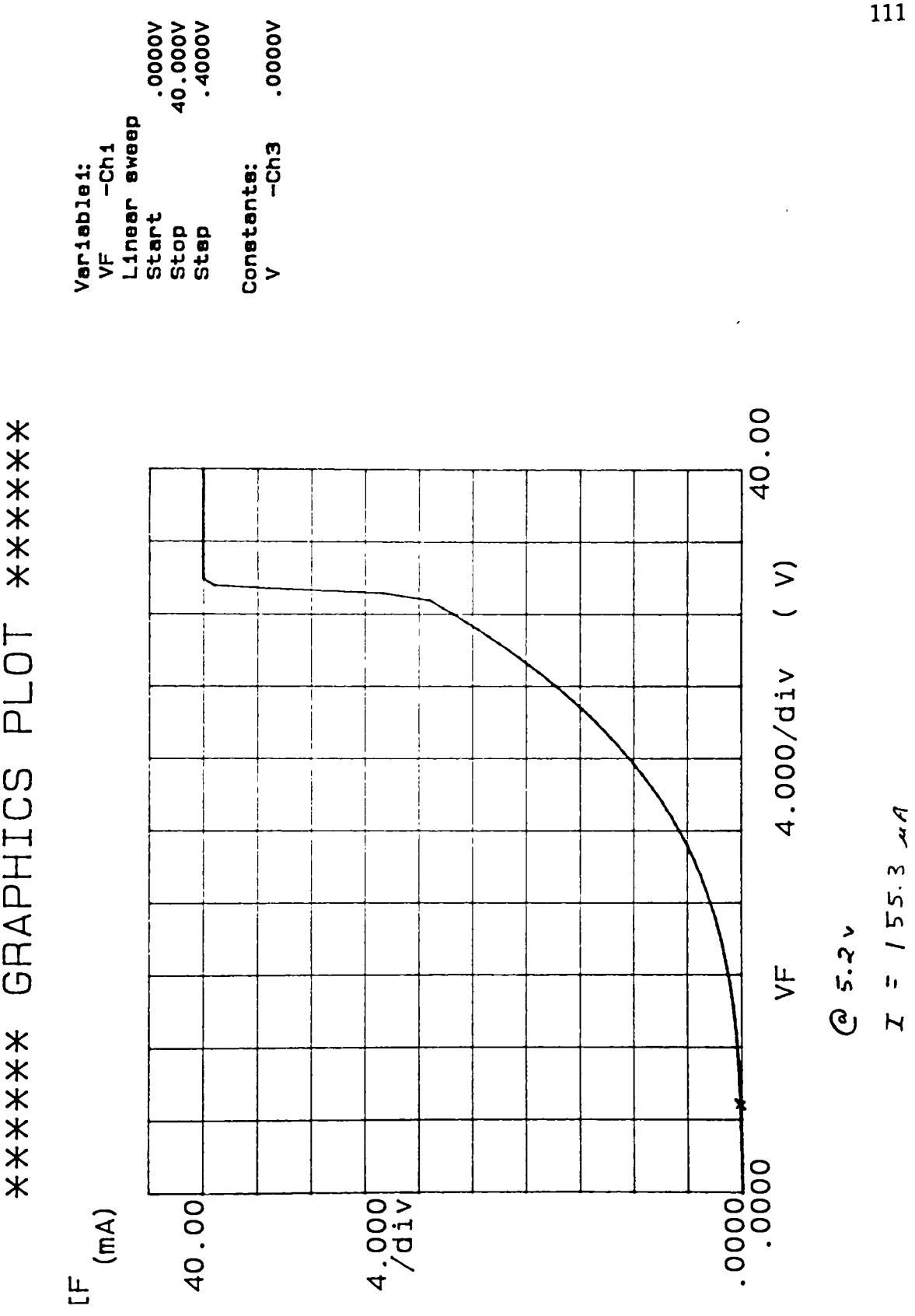
MOS #2, medium field plate overlap, breakdown voltage without passivation

Fig 5.8



MOS #3, longest field plate overlap, breakdown voltage without passivation

Fig 5.9

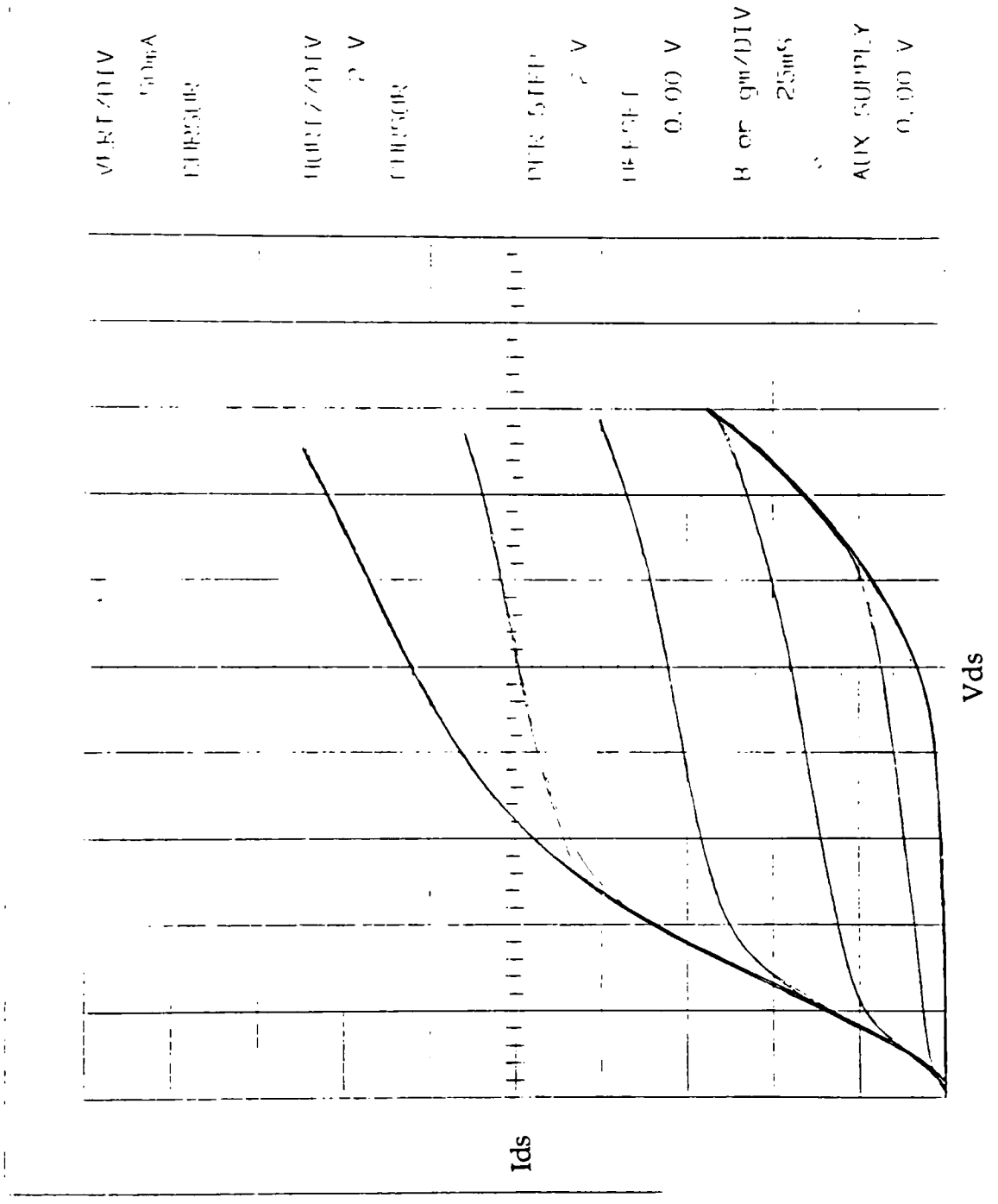


Power MOS breakdown voltage with passivation

Fig 5.10

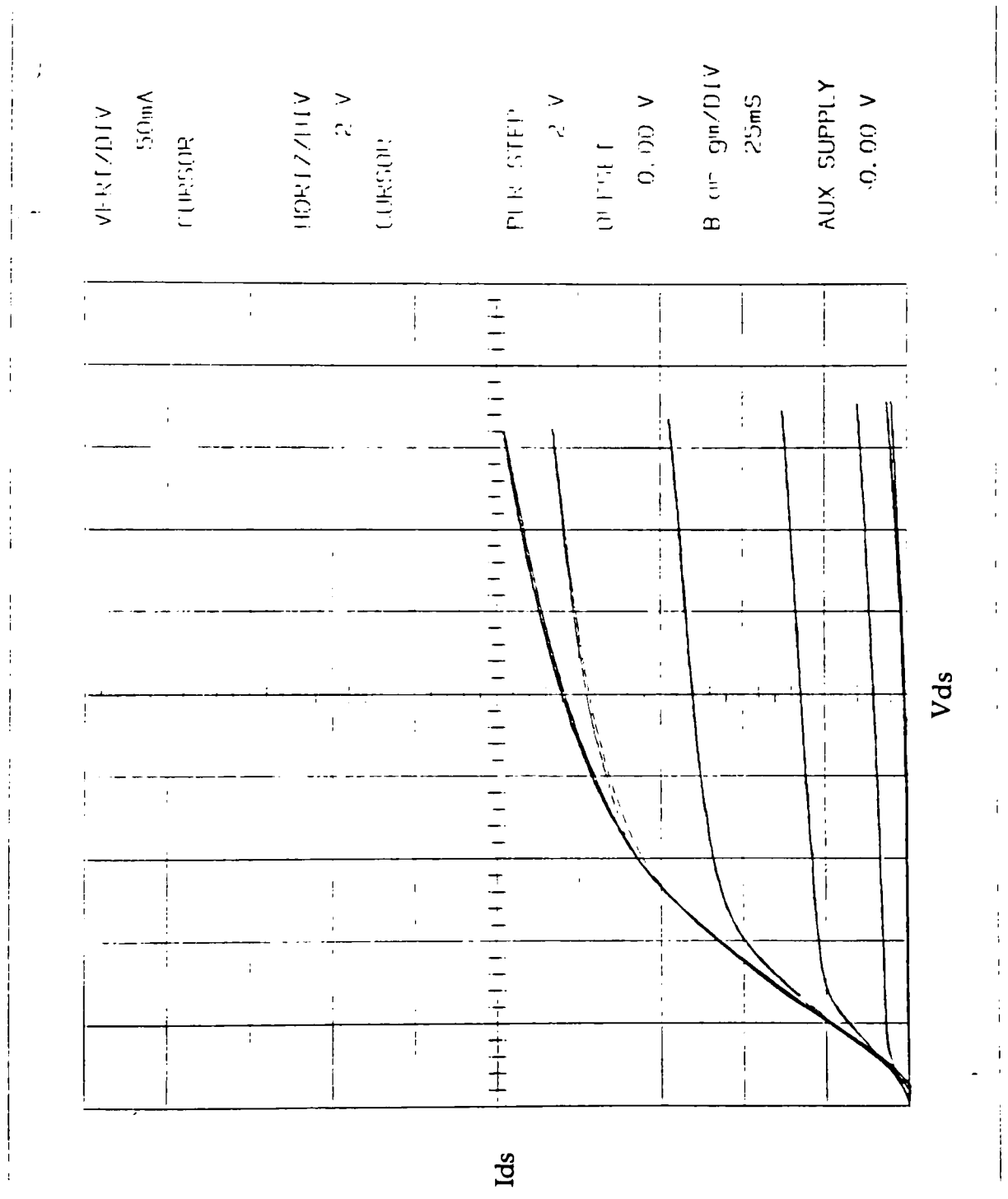
The initial tests on the 370 were to determine the current handling capability of the device. The best power MOS device showed a current of approximately 600mA under a gate voltage of 12 volts. More typical devices could handle currents of approximately 300mA. (see fig 5.11 and 5.12 for typical I-V characteristic curves) The breakdown voltages of the devices were tested under power limitations to prevent thermal destruction. The largest observed breakdown voltage was approximately 60 volts. Typical breakdown voltages were around 35 volts. Fig 5.13 shows the breakdown of a typical device. The device with the largest transconductance and breakdown voltage was destroyed during breakdown voltage testing. Fig 5.14 and Fig 5.15 are pictures of the device following the destructive testing and show the thermally damaged regions. The damage occurred as a result of current crowding at the right angle corners to the source contact pad. This should serve as a good example of the need for rounded corners.

Fig 5.11 shows that there is a larger drain to source current with a gate voltage of 0V than with a gate voltage of 2V. This is unexpected, as Vgs increases a channel forms and the current flow through the device should increases. It is spected that there is a significant leakage through the gate and as the gate voltage increases up to threshold point, the potential on the gate could divert the current through the oxide. After the threshold voltage the current through the device is large enough so that the lose through the gate is not seen.



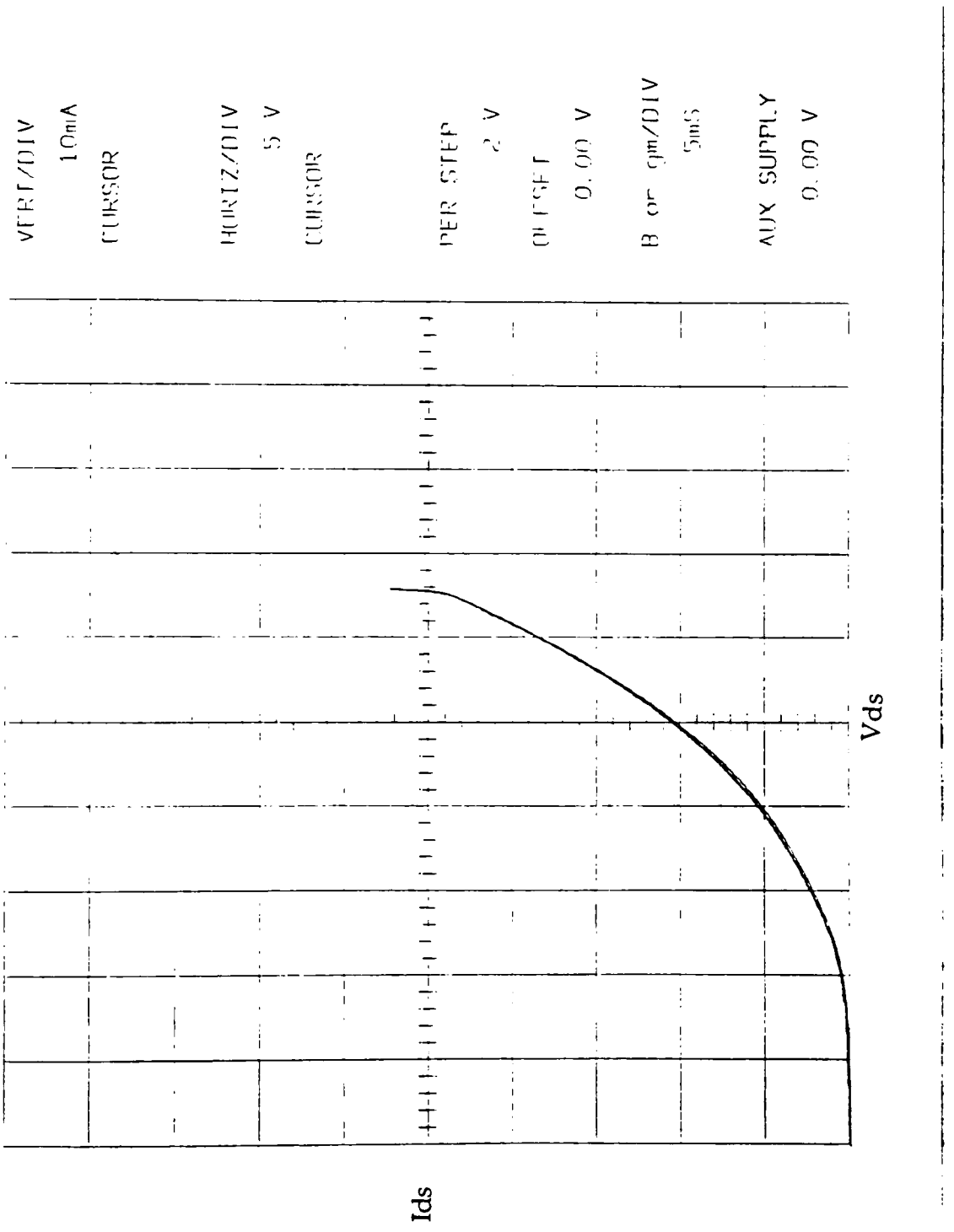
Ids vs Vds for MOS #1, D4, with a floating well

Fig 5.11



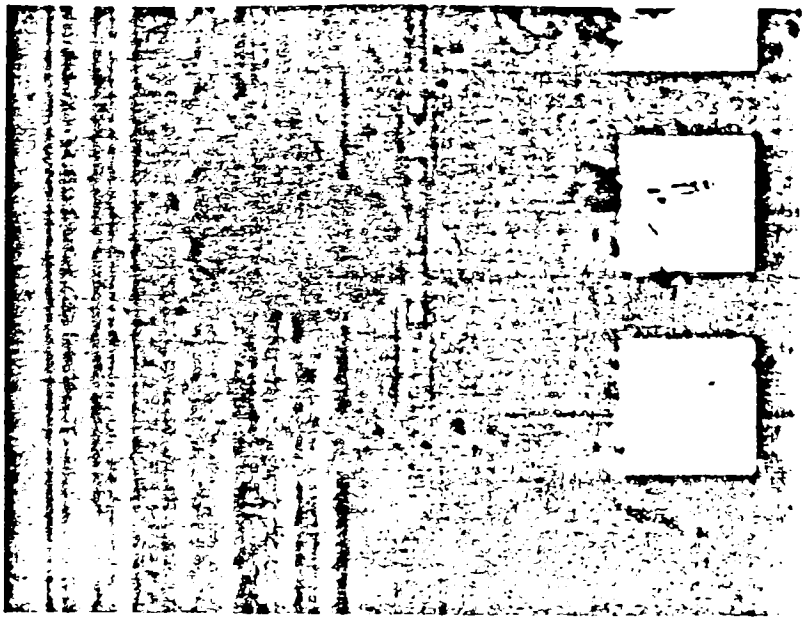
Ids vs Vds for MOS #1, D2, with a floating well

Fig 5.12



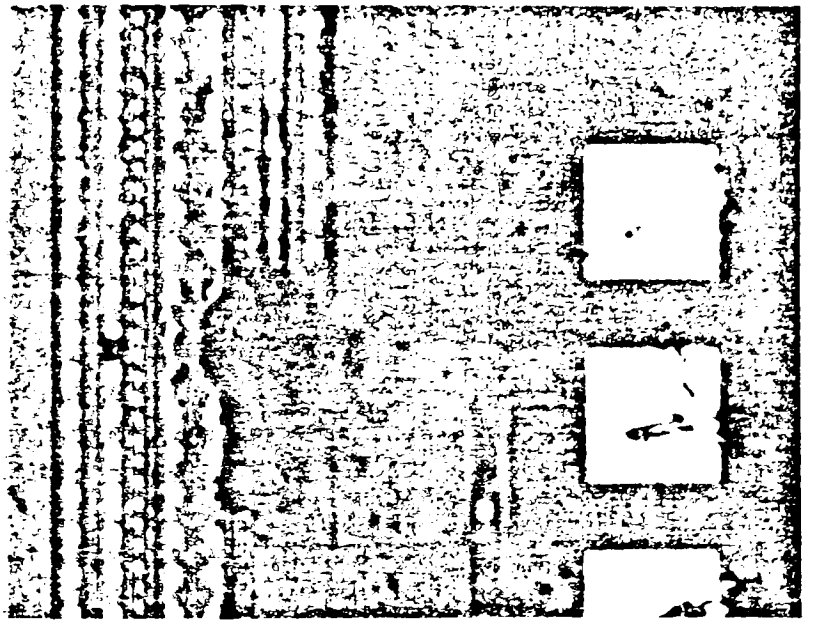
Breakdown Voltage curve for D2 with a floating well

Fig 5.13



Picture showing the thermally damaged region after destructive testing

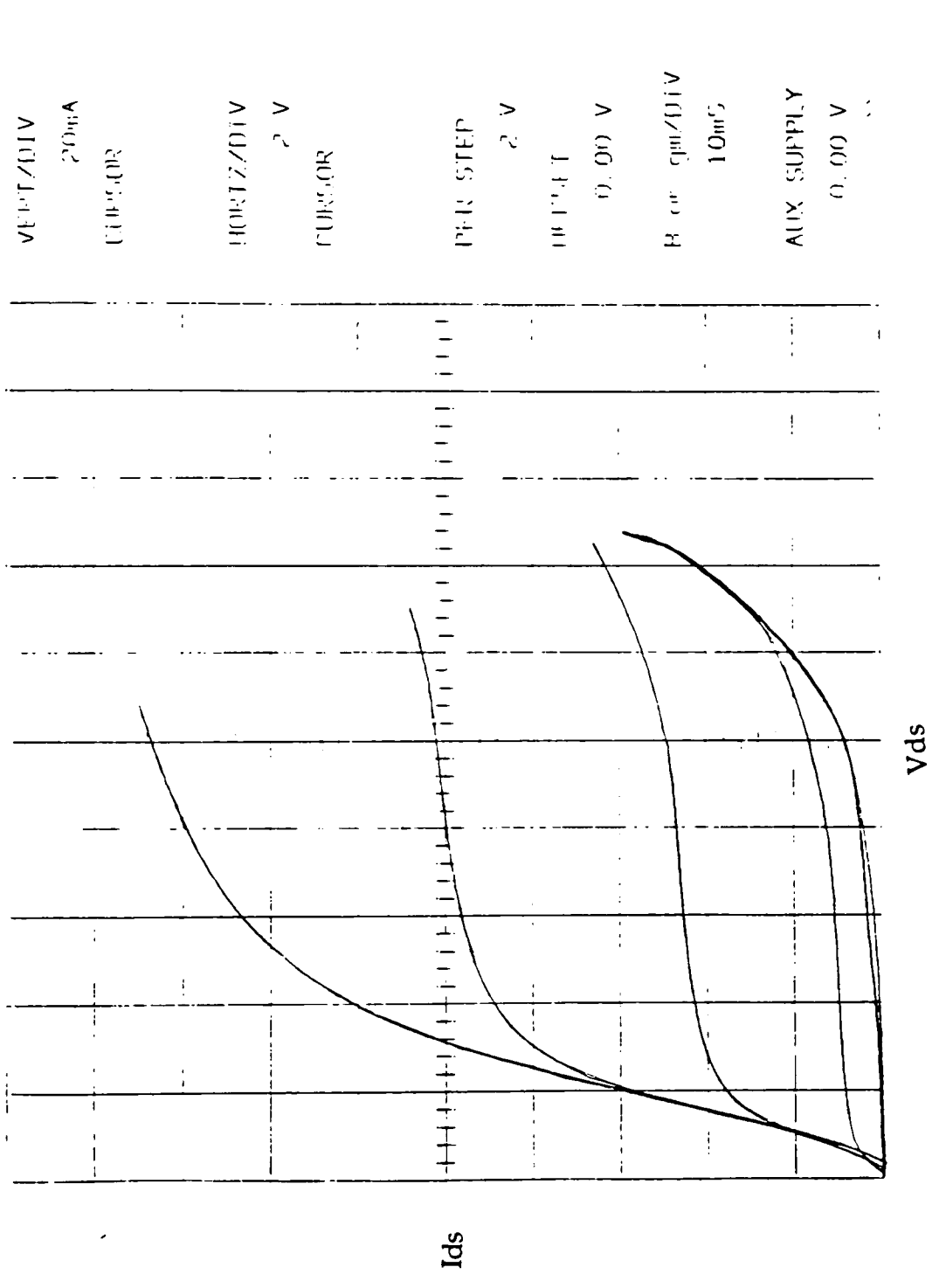
Fig 5.14



Picture showing the thermally damaged region after destructive testing

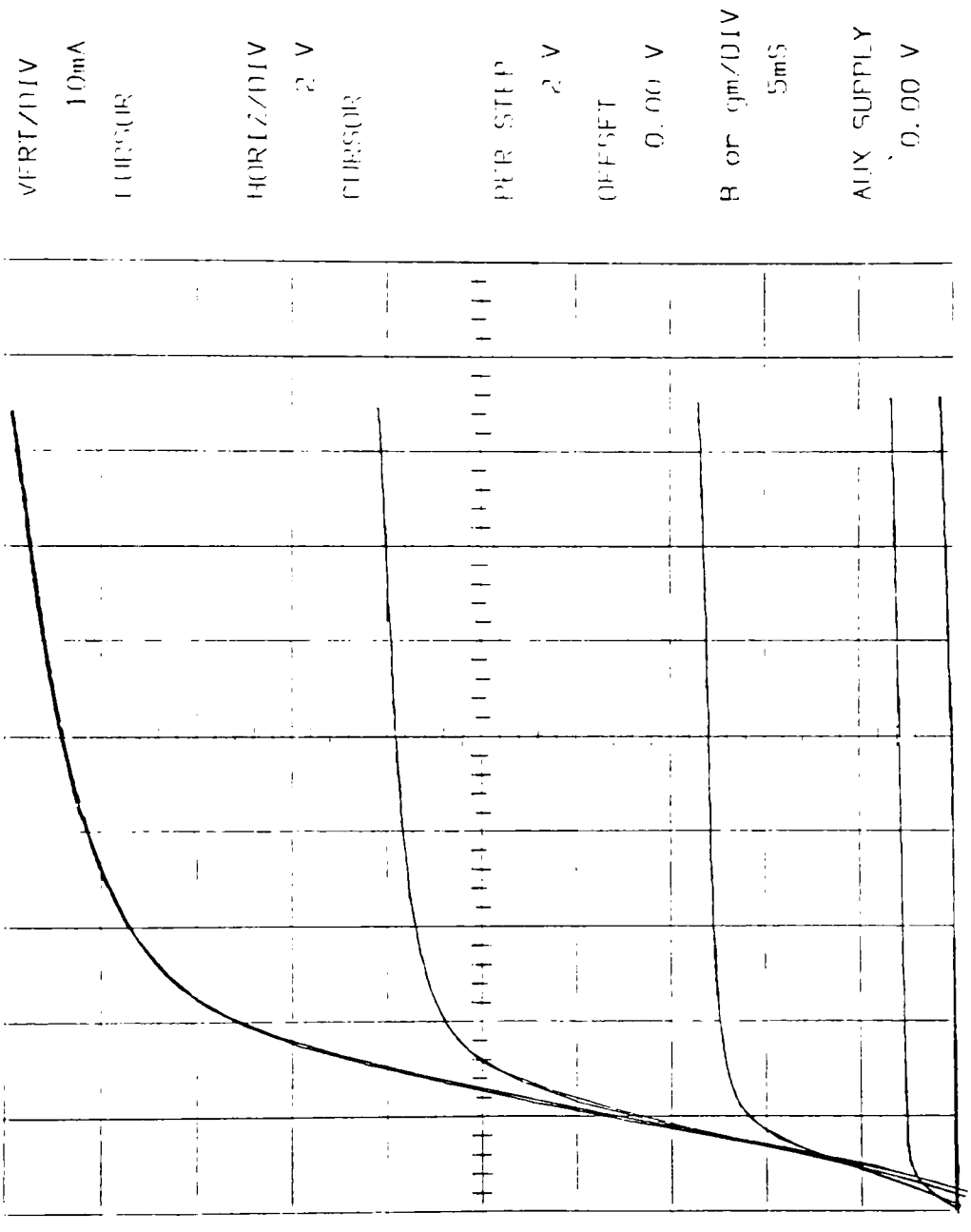
Fig 5.15

The effect of grounding the well was then studied. By grounding the well a reduction in current of approximately 50% was encountered. Fig 5.16 and 5.17 show the same device as Fig 5.11 and fig 5.12 but with the well grounded. The breakdown voltage was also tested with the grounded well and a reduction of approximately 10% was seen. Fig 5.18 shows the breakdown of the same device as in Fig 5.13 but with a grounded well.



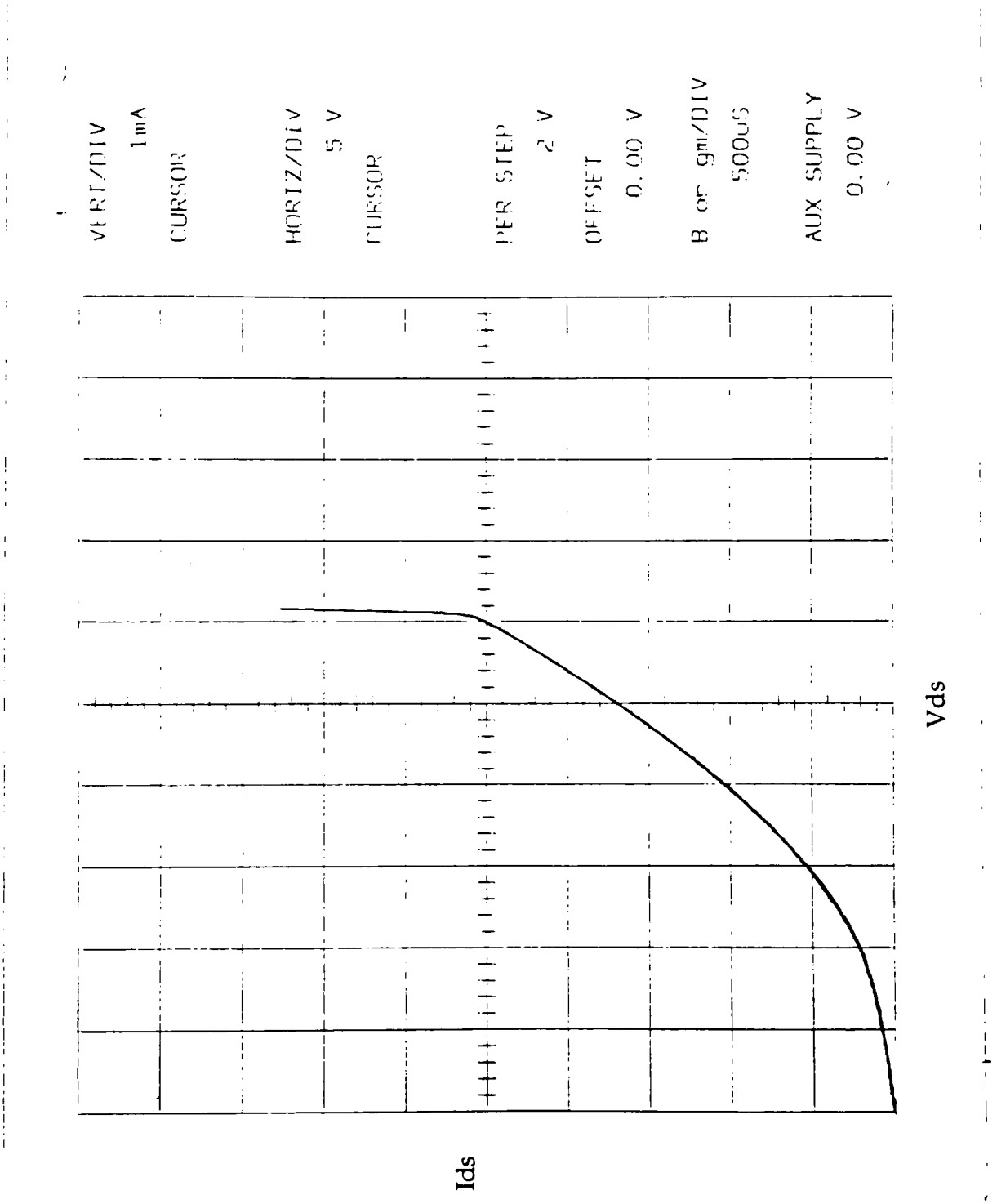
Ids vs Vds for MOS #1, D4, with a grounded well

Fig 5.16



Ids vs Vds for MOS #1, D2, with a grounded well

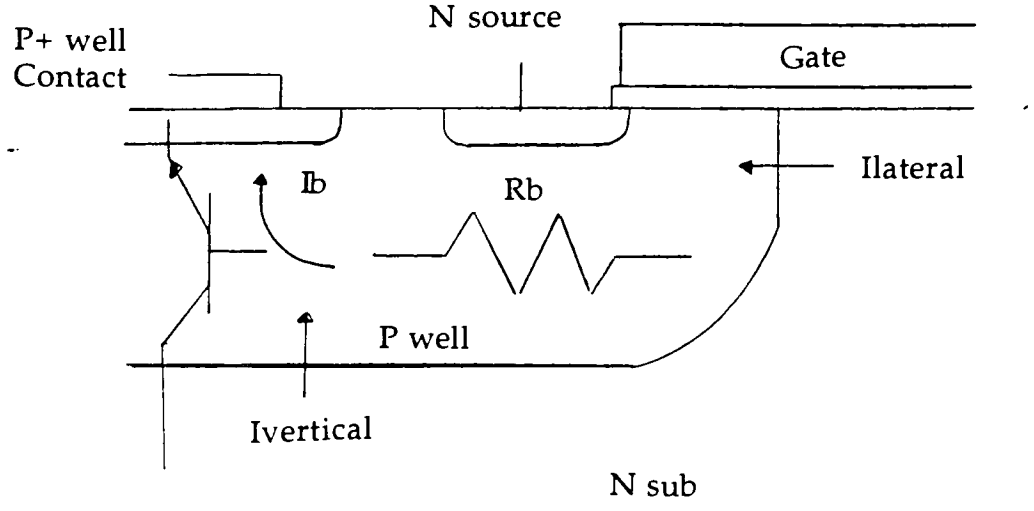
Fig 5.17



Breakdown Voltage curve for D2 with a grounded well

Fig 5.18

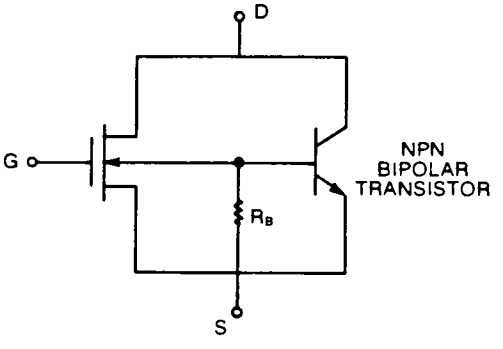
The effect of the increased current, when testing with the well floating, is attributed to the turning on of the parasitic vertical NPN BJT. Fig 5.19 shows a cross section of the Power MOS structure, indicating are the MOS and BJT actions.



Cross section of MOSFET showing possible parasitic BJT

Fig 5.19

Redrawing the Power NMOSFET with circuit symbols results in Fig 5.20



Circuit equivalent of parasitic BJT and lateral well resistance in MOSFET

Fig 5.20

Referring to Fig 5.19, the holes that are forces away from a positive voltage tend to migrate to the P+ well contact. With the well grounded, only the laterally migrating holes cause a current through Rb under the source. If

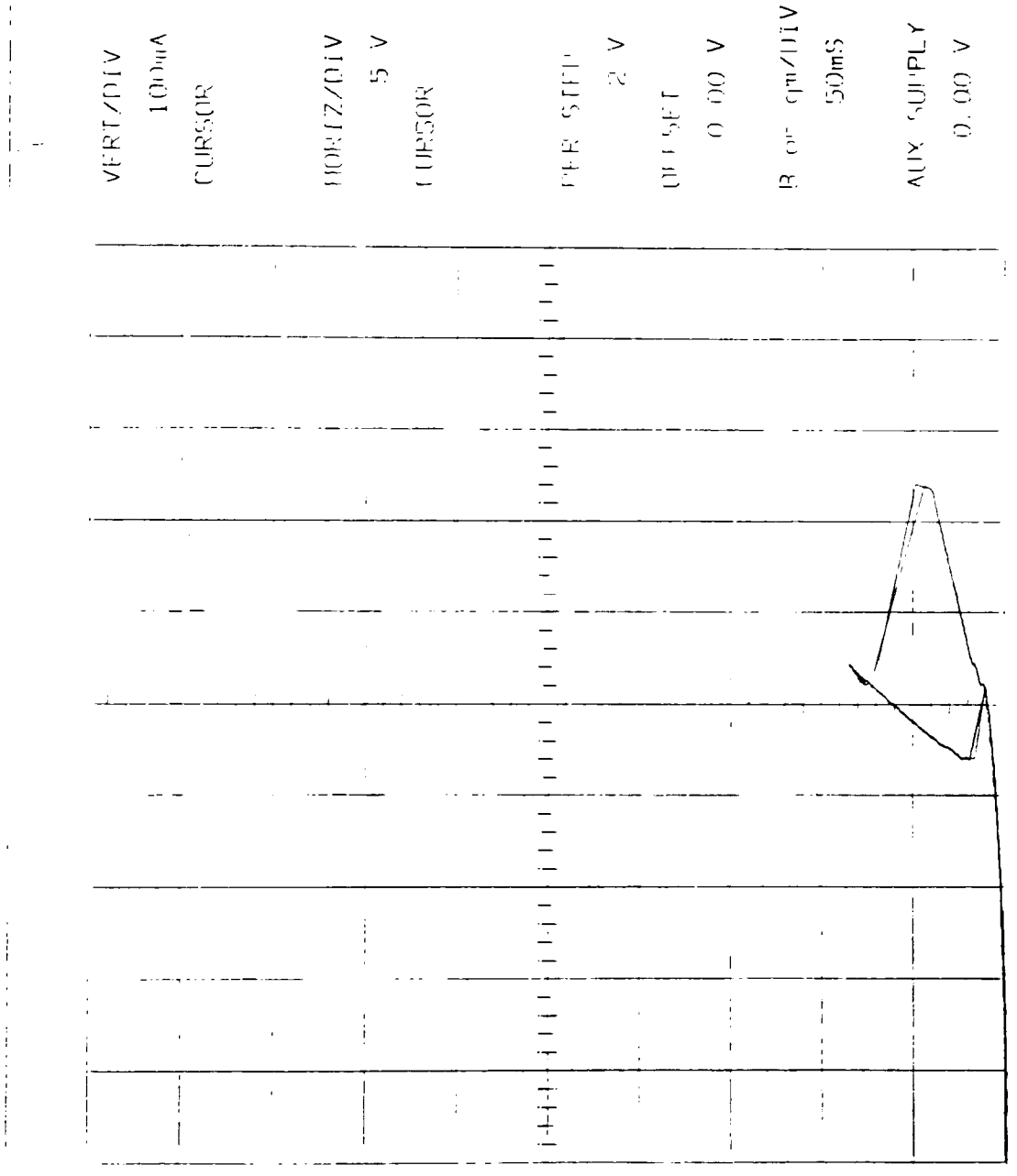
the voltage under the source is large enough to forward bias the well/source junction, a BJT breakdown will occur. This biasing will inject holes into the source, similar to an emitter-base diode, resulting in a current flow from the source. With a grounded well, the biasing voltage can only appear at the source end farthest from the well contact. Holes having a shorter distances to travel to reach the well contact produce a smaller voltage. For a floating well, all of the holes must reach the N+ source contact. This results in a biasing voltage under the entire source. With the entire source acting like an emitter-base diode, a larger current flow from the source will occur. This explains why the floating well tests showed a much larger current than that of the grounded well. This process is effect by the gate voltage directly. The relationship between the gate voltage and the potential of the silicon is

$$Vgb = \Psi ox + \Psi s + \Phi ms \qquad \text{Eq 5.1.1}$$

Vgb is the voltage from gate to bulk, Ψox is the potential drop across the oxide, Ψs is the potential drop across the silicon and Φms is the gate-to-bulk work function difference. As the gate voltage is increased, the silicon potential would also increase. This accounts for the gate control of the NPN transistor. By increasing the well doping, Rb is reduce and the diode bias is decreased.

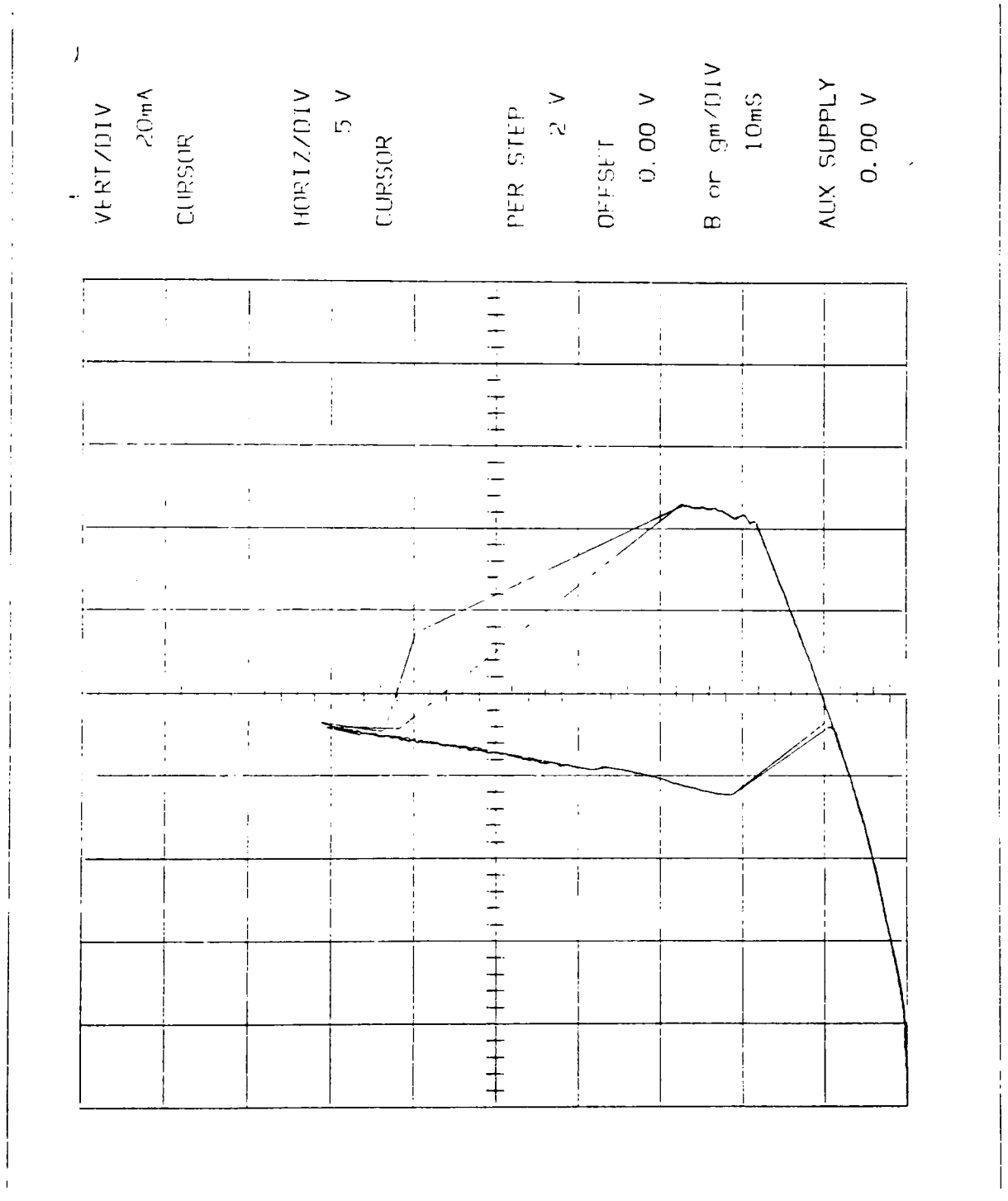
In several devices a snap back type breakdown curve was encountered. Fig 5.21 and Fig 5.22 show this. Referring to Fig 2.4, the similarity of the snap back curve with negative resistance is seen. Applying the reasoning above, the snap back occurs when the leakage current is large enough to forward bias the well/source junction. Calculating the well resistance resulted in an approximate value of 6Ω. The leakage current where the snap back occurs is

about 100mA. This would produce a voltage of 0.6V which is near the voltage needed to forward bias the PN junction.



Current vs voltage curve for MOS #1, D2, showing BJT breakdown action

Fig 5.21



Current vs voltage curve for MOS #1, D5, showing BJT breakdown action

Fig 5.22

6. Future Development

From the data obtained in the first device fabrication, SUPREM 4 and MEDICI should be updated for non-idealities.

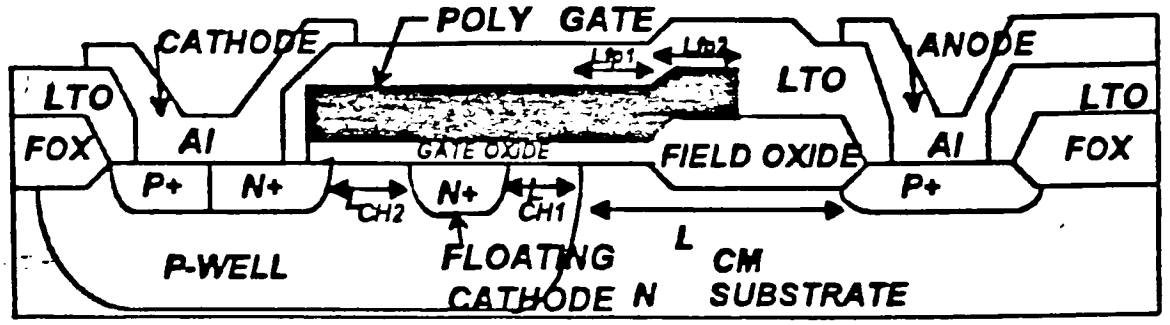
The use of the Power_design layers in I.C. Station for the device design will result in alterations in the mask making procedure. Table 6.1 shows the needed changes in bold.

IC Level	IC Name	Reticle Level	Reticle Name	Dark or Clear Field Mask
1	**Drift**	**4**	**Adj Block**	**Clear**
2	P Well	1	Well	Dark
3	Active	2	Active	Clear
4	N+ Select	7	N+ S/D	Dark
2 , 3*		3	Channel Stop	Dark
1 , 5**		**5**	**Vt Adj**	**Dark**
5	P+ Select	8	P+ S/D	Dark
6	Poly	6	Poly	Clear
7	Contact_A	9***	CC	Dark
8	Contact_P	9***	CC	Dark
9	Metal	10	Metal	Clear
10	Via	11	Via	Dark

* IC Levels 2 and 3 are combined as [Inv2 ORed 3] to obtain Reticle Level 3
** IC Levels 1 and 5 are combined as [1 ORed inv5] to obtain Reticle Level 5
*** IC Levels 7 and 8 are 'ORed' together to produce the Reticle Level 9

Table 6.1

An additional lithography step is needed for the threshold adjust block. This would come prior to the first threshold adjust implant. The IC layer, Drift, should be placed from the end of the drain region to the expected end of the well lateral diffusion.



Cross section of the Lateral Emitter Switched Thyristor, LEST

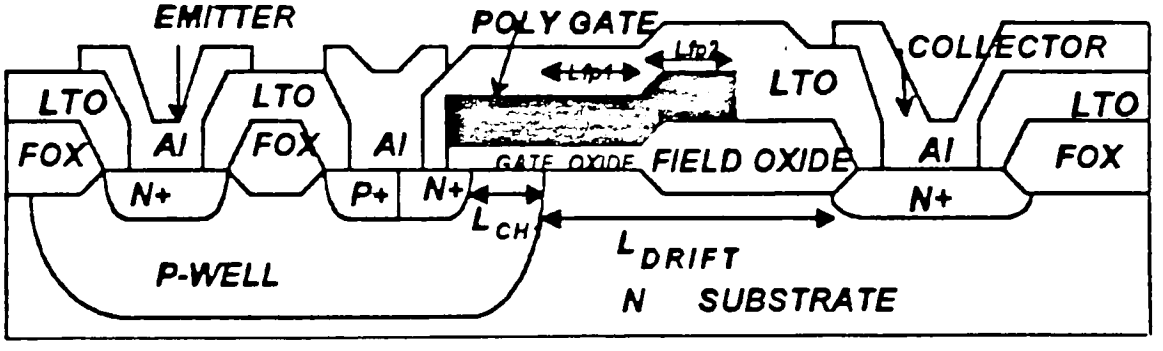
Fig 6.2

With the correction to the P+ mask, the IGBT should be fabricated again. The effect of the P+ drain on the conductivity of the drift region through minority carrier injection from the drain should be investigated for increased current handling.

With the power devices designed and operational, simple control circuits should be designed and fabricated using them. Based on this information protection techniques can be implemented and Intelligent Power Integrated Circuits produced.

The relatively low breakdown voltage of the device indicates that a longer drift region is worth studying. With the corrections to the layout, the device should be fabricated with an increased drift region of 15μm. This should provide more information on the breakdown voltage. The longer drift region should insure that the depletion region does not extend into the drain and the smallest electric field possible is produced.

Other related power devices such as the Insulated Base Transistor, IBT, and the Lateral Emitter Switched Thyristor, LEST, shown in Fig 6.1 and Fig 6.2, should also be studied. Their current handling capability, on resistance and breakdown voltage ratings are of interest in determining the most suitable power device for a given application.



Cross section of the Insulated Base Transistor, IBT

Fig 6.1

7. Conclusion

Power Integrated Circuits are being utilized in many areas especially power supplies, auto electronics and display drivers. As the isolation techniques between high and low power components improve, the applications of these devices will increase. The ability of these devices to decrease component size, reduce power consumption and improve performance over their discrete counter parts insures their role in future electronics.

The initial work for PIC development involved the design of a lateral Power MOSFET and IGBT. The drift region and field plate overlap were investigated for their effects on the breakdown voltage and on resistance. The results from this work indicate that these power devices are feasible and PIC development is possible at R.I.T. The challenge of optimizing the properties studied above to produce application specific power devices is one area that should be addressed in the future. Future work should also include the study of isolation methods for devices, the design of mixed component circuits and the development of other power components for PIC applications.

The relatively recent development of PICs allow for many improvements to current technology and provides vast opportunities for new technology development. As this field matures expect a redefinition of I.C. electronics and a evolution in I.C. applications.

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Appendix A

Simulation for NMOS power device

Ray Talacka
7/5/94

```
ilename            PWR1.inp
iles used          NONE
iles created       PWRBASE.str

nitialize the structure and set up grid

'ION      DEVICE=x
JE        X LOCATION=0 SPACING=.75
JE        X LOCATION=7 SPACING=.4
JE        X LOCATION=9 SPACING=.2
JE        X LOCATION=11 SPACING=.4
JE        X LOCATION=16 SPACING=.2
NE        X LOCATION=22 SPACING=.4
NE        X LOCATION=24 SPACING=.7
NE        X LOCATION=30 SPACING=1.0
NE        Y LOCATION=0 SPACING=.075
NE        Y LOCATION=1 SPACING=.2
NE        Y LOCATION=3.5 SPACING=.4
NE        Y LOCATION=8 SPACING=.2
NE        Y LOCATION=10 SPACING=.8
IMINATE COLUMNS Y.MIN=8
IMINATE ROWS Y.MIN=8
SH        GRID.FAC=1
ITIALIZE RATIO=1.5 <100> ROT.SUB=0.0 PHOSPHOR=6e14
ELECT     TITLE="Power NMOS Initial Grid"
OT.2D     GRID SCALE X.MAX=30 Y.MAX=10

     Initial well masking and alignment oxidation

ETHOD     VERTICAL
IFFUSION TIME=35 TEMPERAT=1100 WETO2
ELECT     TITLE="Alignment Oxide"
LOT.2D    GRID SCALE X.MAX=30 Y.MAX=10
OLOR      COLOR=7 SILICON
OLOR      COLOR=3 OXIDE

TCH       OXIDE LEFT P1.X=11

ELECT     TITLE="Well Implant"
LOT.2D    GRID SCALE X.MAX=30 Y.MAX=10
OLOR      COLOR=7 SILICON
OLOR      COLOR=3 OXIDE
;
MPLANT    BORON DOSE=4e12 ENERGY=50 PEARSON RP.EFF
IFFUSION TIME=240 TEMPERAT=1125 DRYO2
IFFUSION TIME=960 TEMPERAT=1125 INERT
$
$     Plot of well diffusion
$
SELECT    Z=log10(boron-6e14) TITLE="Well Porfile (vertical @ x=10u)"
PLOT.1D   X.VALUE=10 LINE.TYP=1 COLOR=1 LEFT=0 RIGHT=10 BOTTOM=13 TOP=16 +
 X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4
SELECT    Z=log10(boron) TITLE="Well Drive-In - 1e14 to 1e16"
PLOT.2D   Y.MAX=10 X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 +
 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
```

```
COLOR      COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
FOREACH    x(14 to 16 setp .5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
ETCH       OXIDE ALL
$
$      LOCOS Process
$
DIFFUSION  TIME=50 TEMPERAT=1100 DRYO2
DEPOSITION NITRIDE THICKNES=.15 SPACES=1
$
SELECT     Z=log10(boron) TITLE="Pad Oxide and Nitride"
PLOT.2D    GRID SCALE X.MAX=30 Y.MAX=10
COLOR      COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR      COLOR=2 NITRIDE
FOREACH    x(14 to 16 setp .5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
ETCH       NITRIDE START X=19 Y=0
ETCH       NITRIDE CONTINUE X=25 Y=0
ETCH       NITRIDE CONTINUE X=25 Y=1
ETCH       NITRIDE DONE X=19 Y=1
ETCH       OXIDE START X=19 Y=0
ETCH       OXIDE CONTINUE X=25 Y=0
ETCH       OXIDE CONTINUE X=25 Y=1
ETCH       OXIDE DONE X=19 Y=1
$
$      Plot of Boron Concentration after SiN Deposit
$
SELECT     Z=log10(boron) TITLE="Negative of Active Area"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR      COLOR=7    SILICON
COLOR      COLOR=3 OXIDE
COLOR      COLOR=2 NITRIDE
FOREACH    x(14 to 16 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.2 SPACES=1
IMPLANT    PHOSPHOR DOSE=8e13 ENERGY=100 PEARSON RP.EFF
ETCH       PHOTORES ALL
DIFFUSION TIME=210 TEMPERAT=1100 WETO2
$
$      Plot of Channel Stop Implant and Oxide Growth
$      Channel Stop Implant should have no effect
$
SELECT     Z=log10(boron) TITLE="Well after Channel Stop and Field Oxidation"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR      COLOR=7    SILICON
COLOR      COLOR=3 OXIDE
COLOR      COLOR=2    NITRIDE
FOREACH    x(14 to 16 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
```

```
$
ETCH       OXIDE OLD.DRY THICKNES=.05
ETCH       NITRIDE ALL
ETCH       OXIDE OLD.DRY THICKNES=.1
$
SELECT     Z=log10(boron) TITLE="Active Area"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR      COLOR=7    SILICON
COLOR      COLOR=3 OXIDE
FOREACH    x(14 to 16 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
$      KOOI Process
$
DIFFUSION TIME=15 TEMPERAT=1000 WETO2
$
$      Layers check
$
SELECT     Z=doping
PRINT.1D   X.VALUE=28 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=5 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=20 LAYERS
$
IMPLANT    BORON DOSE=5.3e11 ENERGY=35 PEARSON RP.EFF
DEPOSITION PHOTORES POSITIVE THICKNES=1.2 SPACES=1
ETCH       PHOTORES START X=2 Y=3
ETCH       PHOTORES CONTINUE X=30 Y=3
ETCH       PHOTORES CONTINUE X=30 Y=-3
ETCH       PHOTORES DONE X=2 Y=-3
$
SELECT     Z=log10(boron) TITLE="Vt Adjust Implant Area"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR      COLOR=7    SILICON
COLOR      COLOR=3 OXIDE
COLOR      COLOR=6 PHOTORES
FOREACH    x(14 to 16 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
IMPLANT    BORON DOSE=4e12 ENERGY=35 PEARSON RP.EFF
ETCH       PHOTORES ALL
ETCH       OXIDE OLD.DRY THICKNES=.15
$
$      Plot of Threashold Adjust Implants
$
SELECT     Z=log10(boron) TITLE="Boron after N+ Vt Adjust (e14 to e18)"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR      COLOR=7    SILICON
COLOR      COLOR=3 OXIDE
FOREACH    x(14 to 18 step 1)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
```

```
$
$      Save File for Device Portion of Simulation
$
SAVEFILE  OUT.FILE=PWRBASE.str SCALE=1.0
```

```
$ Simulation for  NMOS power device
$
$ Ray Talacka
$ 7/5/94
$
$ filename      MOS_S4.inp
$ fileused       PWR15.str
$ filecreated  MOS_DEV_S4.str
$
$ Initialize the structure
$
INITIALIZE IN.FILE=PWR15.str SCALE=1.0
OPTION     DEVICE=x
$
$     Growth of gate oxide and poly gate
$
DIFFUSION TIME=12 TEMPERAT=900 T.FINAL=1100 DRYO2
DIFFUSION TIME=35 TEMPERAT=1100 DRYO2
DIFFUSION TIME=18 TEMPERAT=1100 T.FINAL=1000 DRYO2
$
SELECT     Z=doping
PRINT.1D   X.VALUE=32 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=5 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=25 LAYERS
$
SELECT     Z=log10(boron) TITLE="Gate Oxide"
PLOT.2D    X.MAX=35 Y.MAX=10 SCALE X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 +
 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1 GRID L.GRID=1 C.GRID=1
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
DEPOSITION POLYSILI THICKNES=.6 SPACES=1
$
SELECT     Z=log10(boron) TITLE="Poly Deposition"
PLOT.2D     GRID SCALE X.MAX=30 Y.MAX=10
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
DEPOSITION OXIDE THICKNES=.3 SPACES=1 PHOSPHOR=5e20
DIFFUSION TIME=10 TEMPERAT=900 INERT
ETCH       OXIDE TRAPEZOI THICKNES=.3
ETCH       POLYSILI TRAPEZOI THICKNES=.05
ETCH       POLYSILI LEFT P1.X=9
ETCH       POLYSILI RIGHT P1.X=20
$
SELECT     Z=doping
PRINT.1D   X.VALUE=32 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=5 LAYERS
```

```
SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=25 LAYERS
$
$      Plot of poly gate structure
$
SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS
SELECT     Z=log10(boron) TITLE="Poly Gate Structure"
PLOT.2D    X.MAX=35 Y.MAX=10 SCALE X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 +
 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1 GRID L.GRID=1 C.GRID=1
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
$      P+  implant
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.2 SPACES=1
ETCH       PHOTORES RIGHT P1.X=1
ETCH       OXIDE TRAPEZOI THICKNES=.15
$
SELECT     Z=log10(boron) TITLE="P+ Implant Area"
PLOT.2D     GRID SCALE X.MAX=30 Y.MAX=10
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
COLOR      COLOR=6 PHOTORES
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
IMPLANT    BF2 DOSE=1e15 ENERGY=120 PEARSON RP.EFF
ETCH       PHOTORES ALL
$
SELECT     Z=doping
PRINT.1D   X.VALUE=32 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=5 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=25 LAYERS
$
$      Plot after P+ implant
$
SELECT     Z=log10(boron) TITLE="P+ Implant"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
$      N+ implant for source and drain
```

```
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.2 SPACES=1
ETCH       PHOTORES RIGHT P1.X=2
$
SELECT     Z=log10(boron) TITLE="N+ Implant Area"
PLOT.2D    X.MAX=35 Y.MAX=10 SCALE X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 +
 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1 GRID L.GRID=1 C.GRID=1
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR      ; COLOR=2 POLY
COLOR      COLOR=6 PHOTORES
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
IMPLANT    PHOSPHOR DOSE=4e15 ENERGY=150 PEARSON RP.EFF
ETCH       PHOTORES ALL
$
SELECT     Z=doping
PRINT.1D   X.VALUE=32 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=5 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=25 LAYERS
$
$      Plot of N+ implant
$
SELECT     Z=log10(phosphorus) TITLE="N+ Implant"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=3 COLOR=3
END
SELECT     Z=log10(boron)
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
$
$      Final processing of contact cuts and Al deposit
$
DEPOSITION OXIDE THICKNES=.6 SPACES=1
DIFFUSION TIME=30 TEMPERAT=950 INERT
ETCH       OXIDE LEFT P1.X=1
ETCH       OXIDE RIGHT P1.X=33
ETCH       OXIDE START X=3 Y=-1
ETCH       OXIDE CONTINUE X=5 Y=-1
ETCH       OXIDE CONTINUE X=5 Y=1
ETCH       OXIDE DONE X=3 Y=1
$
SELECT     Z=log10(boron) TITLE="Contact Cuts"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
```

```
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
SELECT     Z=log10(phosphorus)
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=3 COLOR=3
END
$
DEPOSITION ALUMINUM THICKNES=.75 SPACES=1
$
SELECT     Z=log10(boron) TITLE="Aluminum Deposition"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
COLOR      COLOR=4 ALUMINUM
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
SELECT     Z=log10(phosphorus)
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=3 COLOR=3
END
$
ETCH       ALUMINUM START X=7 Y=0
ETCH       ALUMINUM CONTINUE X=30 Y=0
ETCH       ALUMINUM CONTINUE X=30 Y=-3
ETCH       ALUMINUM DONE X=7 Y=-3
ETCH       ALUMINUM START X=1.1 Y=0
ETCH       ALUMINUM CONTINUE X=2.9 Y=0
ETCH       ALUMINUM CONTINUE X=2.9 Y=-3
ETCH       ALUMINUM DONE X=1.1 Y=-3
$
$      Plot of final structure
$
SELECT     Z=log10(boron) TITLE="Final NMOS Power Device"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
COLOR      COLOR=4 ALUMINUM
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=1 COLOR=1
END
SELECT     Z=log10(phosphorus)
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=x LINE.TYP=3 COLOR=3
END
SELECT     Z=log10(boron) TITLE="Final Well Profile(vertical)"
PLOT.1D    X.VALUE=11 LINE.TYP=2 COLOR=2 BOTTOM=13 TOP=20 X.SIZE=0.25 +
 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4
SELECT     Z=log10(phosphorus)
PLOT.1D    X.VALUE=11 LINE.TYP=1 COLOR=1 ^AXES ^CLEAR
SELECT     Z=log10(phosphorus) TITLE="Final Source Profile(vertical)"
PLOT.1D    X.VALUE=5 LINE.TYP=1 COLOR=1 BOTTOM=13 TOP=20 X.SIZE=0.25 +
 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4
SELECT     Z=log10(boron)
PLOT.1D    X.VALUE=5 LINE.TYP=2 COLOR=2 ^AXES ^CLEAR
```

```
SELECT     Z=log10(phosphorus) TITLE="Final Drain Profile(vertical)"
PLOT.1D    X.VALUE=33 LINE.TYP=1 COLOR=1 BOTTOM=13 TOP=20 X.SIZE=0.25 +
 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4
SELECT     Z=log10(boron)
PLOT.1D    X.VALUE=33 LINE.TYP=2 COLOR=2 ^AXES ^CLEAR
SELECT     Z=log10(Phosphorus) TITLE="Final Drift Region Profile(vertical)"
PLOT.1D    X.VALUE=20 LINE.TYP=1 COLOR=1 BOTTOM=13 TOP=20 X.SIZE=0.25 +
 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4
SELECT     Z=log10(boron)
PLOT.1D    X.VALUE=20 LINE.TYP=2 COLOR=2 ^AXES ^CLEAR
$
SELECT     Z=doping
PRINT.1D   X.VALUE=32 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=5 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS
SELECT     Z=doping
PRINT.1D   X.VALUE=25 LAYERS
$
$SAVEFILE   OUT.FILE=MOS_DEV_S4.str SCALE=1.0
STRUCTURE OUT.FILE=MOS_MED15_S4.str SCALE=1.0 MEDICI POLY.ELE
STOP
```

```
            ************************************************************
            ***                    TSUPREM-4 (TM)                    ***
            ***         Version 5.2.4, System H (HP: HP-UX)          ***
            ***               Copyright (C) 1988-1993                ***
            ***        Technology Modeling Associates, Inc.          ***
            ***                  All Rights Reserved                 ***
            ************************************************************

                                8-Nov-94 16:52:43


 Entering source file PWR1_S4.inp.

$                                          Simulation for NMOS power device
$
$                                          Ray Talacka
$                                          7/5/94
$
$ filename            PWR1.inp
$ files used          NONE
$ files created      PWRBASE.str
$
$ Initialize the structure and set up grid
$
OPTION     DEVICE=x
LINE       X LOCATION=0 SPACING=.75
LINE       X LOCATION=7 SPACING=.4
LINE       X LOCATION=9 SPACING=.2
LINE       X LOCATION=11 SPACING=.4
LINE       X LOCATION=16 SPACING=.2
LINE       X LOCATION=22 SPACING=.4
LINE       X LOCATION=24 SPACING=.7
LINE       X LOCATION=30 SPACING=1.0
LINE       Y LOCATION=0 SPACING=.075
LINE       Y LOCATION=1 SPACING=.2
LINE       Y LOCATION=3.5 SPACING=.4
LINE       Y LOCATION=8 SPACING=.2
LINE       Y LOCATION=10 SPACING=.8
ELIMINATE COLUMNS Y.MIN=8
ELIMINATE ROWS Y.MIN=8
MESH       GRID.FAC=1
INITIALIZE RATIO=1.5 <100> ROT.SUB=0.0 PHOSPHOR=6e14
   77 lines in the x direction.
   38 lines in the y direction.
SELECT     TITLE="Power NMOS Initial Grid"
PLOT.2D    GRID SCALE X.MAX=30 Y.MAX=10

   Top of the device is at y=0.00 microns.
   Top axis is at y=-1.00 microns.

$
$     Initial well masking and alignment oxidation
$
METHOD     VERTICAL
DIFFUSION TIME=35 TEMPERAT=1100 WETO2
SELECT     TITLE="Alignment Oxide"
```

```
PLOT.2D     GRID SCALE X.MAX=30 Y.MAX=10

   Top of the device is at y=-0.279 microns.
   Top axis is at y=-1.31 microns.

COLOR       COLOR=7 SILICON
COLOR       COLOR=3 OXIDE
$
ETCH        OXIDE LEFT P1.X=11
$
SELECT      TITLE="Well Implant"
PLOT.2D     GRID SCALE X.MAX=30 Y.MAX=10

   Top of the device is at y=-0.279 microns.
   Top axis is at y=-1.31 microns.

COLOR       COLOR=7 SILICON
COLOR       COLOR=3 OXIDE
$
IMPLANT     BORON DOSE=4e12 ENERGY=50 PEARSON RP.EFF
DIFFUSION TIME=240 TEMPERAT=1125 DRYO2
```

```
*************************************************************
***                    TSUPREM-4 (TM)                     ***
***          Version 5.2.4, System H (HP: HP-UX)          ***
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***                  All Rights Reserved                  ***
*************************************************************

                        5-Nov-94 17:41:18

 Entering source file MOS15_S4.inp.

$ Simulation for  NMOS power device
$
$ Ray Talacka
$ 7/5/94
$
$ filename      MOS_S4.inp
$ fileused       PWR15.str
$ filecreated  MOS_DEV_S4.str
$
$ Initialize the structure
$
INITIALIZE IN.FILE=PWR15.str SCALE=1.0
OPTION    DEVICE=x
$
$     Growth of gate oxide and poly gate
$
DIFFUSION TIME=12 TEMPERAT=900 T.FINAL=1100 DRYO2
DIFFUSION TIME=35 TEMPERAT=1100 DRYO2
DIFFUSION TIME=18 TEMPERAT=1100 T.FINAL=1000 DRYO2
$
SELECT    Z=doping
PRINT.1D  X.VALUE=32 LAYERS

 Num      Material       Top     Bottom  Thickness        Integral
   1         oxide    0.3111     0.4093     0.0982      2.1908e+08
   2       silicon    0.4093    10.0000     9.5907      6.0027e+11

SELECT    Z=doping
PRINT.1D  X.VALUE=5 LAYERS

 Num      Material       Top     Bottom  Thickness        Integral
   1         oxide    0.3959     0.4940     0.0981     -4.8375e+10
   2       silicon    0.4940     5.1290     4.6350      1.5860e+12
   3       silicon    5.1290    10.0000     4.8710      2.4495e+11

SELECT    Z=doping
PRINT.1D  X.VALUE=11 LAYERS

 Num      Material       Top     Bottom  Thickness        Integral
   1         oxide    0.3908     0.4821     0.0913     -2.5423e+10
   2       silicon    0.4821     4.4573     3.9752     -6.7431e+11
   3       silicon    4.4573    10.0000     5.5427      2.7965e+11
```

```
SELECT     Z=doping
PRINT.1D   X.VALUE=25 LAYERS

 Num       Material        Top      Bottom  Thickness         Integral
   1          oxide    -0.1627      0.9012     1.0639       7.4757e+09
   2        silicon     0.9012     10.0000     9.0988       5.8418e+11

$
SELECT     Z=log10(boron) TITLE="Gate Oxide"
PLOT.2D    X.MAX=35 Y.MAX=10 SCALE X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 +
 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1 GRID L.GRID=1 C.GRID=1

   Top of the device is at y=-0.194 microns.
   Top axis is at y=-1.21 microns.

COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=1 COLOR=1
END
$
DEPOSITION POLYSILI THICKNES=.6 SPACES=1
$
SELECT     Z=log10(boron) TITLE="Poly Deposition"
PLOT.2D     GRID SCALE X.MAX=30 Y.MAX=10

   Top of the device is at y=-0.808 microns.
   Top axis is at y=-1.89 microns.

COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=1 COLOR=1
END
$
```

```
DEPOSITION OXIDE THICKNES=.3 SPACES=1 PHOSPHOR=5e20
DIFFUSION TIME=10 TEMPERAT=900 INERT
ETCH      OXIDE TRAPEZOI THICKNES=.3
ETCH      POLYSILI TRAPEZOI THICKNES=.05
ETCH      POLYSILI LEFT P1.X=9
ETCH      POLYSILI RIGHT P1.X=20

*** Warning:  Detached region (area=0.0399977 square microns) removed.

*** Warning:  Detached region (area=2.34845e-05 square microns) removed.

*** Warning:  Detached region (area=2.39079e-05 square microns) removed.
$
SELECT    Z=doping
PRINT.1D  X.VALUE=32 LAYERS

 Num      Material       Top      Bottom  Thickness        Integral
   1         oxide    0.3111      0.4093     0.0982      7.1957e+11
   2       silicon    0.4093     10.0000     9.5907      6.0028e+11

SELECT    Z=doping
PRINT.1D  X.VALUE=5 LAYERS

 Num      Material       Top      Bottom  Thickness        Integral
   1         oxide    0.3959      0.4876     0.0917      7.1295e+11
   2         oxide    0.4876      0.4940     0.0064      3.5093e+09
   3       silicon    0.4940      5.1291     4.6351      1.5779e+12
   4       silicon    5.1291     10.0000     4.8709      2.4494e+11

SELECT    Z=doping
PRINT.1D  X.VALUE=11 LAYERS

 Num      Material       Top      Bottom  Thickness        Integral
   1         oxide   -0.2218     -0.2176     0.0042      3.5024e+12
   2   polysilicon   -0.2176      0.3908     0.6085      6.5715e+15
   3         oxide    0.3908      0.4777     0.0868      5.6395e+11
   4         oxide    0.4777      0.4821     0.0045      1.4918e+09
   5       silicon    0.4821      0.4838     0.0017      1.9423e+06
   6       silicon    0.4838      4.4574     3.9736     -6.6960e+11
   7       silicon    4.4574     10.0000     5.5426      2.7964e+11

SELECT    Z=doping
PRINT.1D  X.VALUE=25 LAYERS

 Num      Material       Top      Bottom  Thickness        Integral
   1         oxide   -0.1627      0.9012     1.0639      7.7880e+11
   2       silicon    0.9012     10.0000     9.0988      5.8418e+11

$
$     Plot of poly gate structure
$
SELECT    Z=doping
PRINT.1D  X.VALUE=11 LAYERS

 Num      Material       Top      Bottom  Thickness        Integral
   1         oxide   -0.2218     -0.2176     0.0042      3.5024e+12
   2   polysilicon   -0.2176      0.3908     0.6085      6.5715e+15
   3         oxide    0.3908      0.4777     0.0868      5.6395e+11
   4         oxide    0.4777      0.4821     0.0045     -1.4918e+09
   5       silicon    0.4821      0.4838     0.0017      1.9423e+06
```

```
   6        silicon     0.4838      4.4574      3.9736      -6.6960e+11
   7        silicon     4.4574     10.0000      5.5426       2.7964e+11
```



```
SELECT     Z=log10(boron) TITLE="Poly Gate Structure"
PLOT.2D    X.MAX=35 Y.MAX=10 SCALE X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 +
 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1 GRID L.GRID=1 C.GRID=1

   Top of the device is at y=-0.794 microns.
   Top axis is at y=-1.87 microns.

COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=1 COLOR=1
END
$
$      P+  implant
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.2 SPACES=1
ETCH       PHOTORES RIGHT P1.X=1
ETCH       OXIDE TRAPEZOI THICKNES=.15
$
SELECT     Z=log10(boron) TITLE="P+ Implant Area"
PLOT.2D     GRID SCALE X.MAX=30 Y.MAX=10

   Top of the device is at y=-0.804 microns.
   Top axis is at y=-1.88 microns.

COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
COLOR      COLOR=6 PHOTORES
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=1 COLOR=1
END
```

```
$
IMPLANT    BF2 DOSE=1e15 ENERGY=120 PEARSON RP.EFF
ETCH       PHOTORES ALL
$
SELECT     Z=doping
PRINT.1D   X.VALUE=32 LAYERS

 Num       Material        Top      Bottom  Thickness        Integral
   1        silicon     0.4093      0.9392     0.5299      -1.0451e+15
   2        silicon     0.9392     10.0000     9.0608       5.5037e+11

SELECT     Z=doping
PRINT.1D   X.VALUE=5 LAYERS

 Num       Material        Top      Bottom  Thickness        Integral
   1        silicon     0.4940      5.1291     4.6351      -2.7004e+14
   2        silicon     5.1291     10.0000     4.8709       2.4494e+11

SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS

 Num       Material        Top      Bottom  Thickness        Integral
   1     polysilicon    -0.2176      0.3908     0.6085       5.7017e+15
   2           oxide     0.3908      0.4777     0.0868       5.6395e+11
   3           oxide     0.4777      0.4821     0.0045       1.4918e+09
   4        silicon      0.4821      0.4838     0.0017       1.9423e+06
   5        silicon      0.4838      4.4574     3.9736      -6.6960e+11
   6        silicon      4.4574     10.0000     5.5426       2.7964e+11

SELECT     Z=doping
PRINT.1D   X.VALUE=25 LAYERS

 Num       Material        Top      Bottom  Thickness        Integral
   1           oxide    -0.0127     -0.0126     0.0000       1.9568e+05
   2           oxide    -0.0126      0.2949     0.3075      -5.6968e+12
   3           oxide     0.2949      0.9012     0.6063       4.0600e+09
   4        silicon      0.9012     10.0000     9.0988       5.8418e+11

$
$      Plot after P+ implant
$
SELECT     Z=log10(boron) TITLE="P+ Implant"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1

   Top of the device is at y=-0.793 microns.
   Top axis is at y=-1.87 microns.

COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17.5 LINE.TYP=1 COLOR=1
```

```
CONTOUR    VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=1 COLOR=1
END
$
$      N+ implant for source and drain
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.2 SPACES=1
ETCH       PHOTORES RIGHT P1.X=2
$
SELECT     Z=log10(boron) TITLE="N+ Implant Area"
PLOT.2D    X.MAX=35 Y.MAX=10 SCALE X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 +
 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1 GRID L.GRID=1 C.GRID=1

   Top of the device is at y=-0.804 microns.
   Top axis is at y=-1.88 microns.

COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
COLOR      COLOR=6 PHOTORES
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=1 COLOR=1
END
$
IMPLANT    PHOSPHOR DOSE=4e15 ENERGY=150 PEARSON RP.EFF
ETCH       PHOTORES ALL
$
SELECT     Z=doping
PRINT.1D   X.VALUE=32 LAYERS

 Num       Material       Top      Bottom  Thickness        Integral
   1        silicon     0.4093      0.5178     0.1085     -1.8534e+14
   2        silicon     0.5178     10.0000     9.4822      3.1327e+15

SELECT     Z=doping
PRINT.1D   X.VALUE=5 LAYERS

 Num       Material       Top      Bottom  Thickness        Integral
   1        silicon     0.4940      0.4940     0.0000     -8.8778e+03
   2        silicon     0.4940      1.0000     0.5060      3.4583e+15
   3        silicon     1.0000      5.1291     4.1291     -1.3086e+12
   4        silicon     5.1291     10.0000     4.8709      2.4494e+11

SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS
```

```
 Num       Material        Top      Bottom  Thickness        Integral
   1    polysilicon    -0.2176      0.3908     0.6085      6.1187e+15
   2          oxide     0.3908      0.4777     0.0868      5.6398e+11
   3          oxide     0.4777      0.4821     0.0045     -1.4917e+09
   4        silicon     0.4821      0.4838     0.0017      1.9423e+06
   5        silicon     0.4838      4.4574     3.9736     -6.6960e+11
   6        silicon     4.4574     10.0000     5.5426      2.7964e+11

SELECT     Z=doping
PRINT.1D   X.VALUE=25 LAYERS

 Num       Material        Top      Bottom  Thickness        Integral
   1          oxide    -0.0127      0.9012     0.9139      4.8624e+15
   2        silicon     0.9012     10.0000     9.0988      5.8418e+11

$
$      Plot of N+ implant
$
SELECT     Z=log10(phosphorus) TITLE="N+ Implant"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1

   Top of the device is at y=-0.793 microns.
   Top axis is at y=-1.87 microns.

COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=14.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=15 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=15.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=16 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=16.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=17 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=17.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=18 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=18.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=19 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=19.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=20 LINE.TYP=3 COLOR=3
END
SELECT     Z=log10(boron)
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=1 COLOR=1
END
```

```
$
$     Final processing of contact cuts and Al deposit
$
DEPOSITION OXIDE THICKNES=.6 SPACES=1
DIFFUSION TIME=30 TEMPERAT=950 INERT
ETCH      OXIDE LEFT P1.X=1
ETCH      OXIDE RIGHT P1.X=33
ETCH      OXIDE START X=3 Y=-1
ETCH      OXIDE CONTINUE X=5 Y=-1
ETCH      OXIDE CONTINUE X=5 Y=1
ETCH      OXIDE DONE X=3 Y=1
$
SELECT    Z=log10(boron) TITLE="Contact Cuts"
PLOT.2D   X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1

   Top of the device is at y=-1.41 microns.
   Top axis is at y=-2.55 microns.

COLOR      COLOR=7 SILICON
COLOR     COLOR=3 OXIDE
COLOR      COLOR=2 POLY
FOREACH x(14 to 20 step 0.5)
CONTOUR   VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=17.5 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR   VALUE=20 LINE.TYP=1 COLOR=1
END
SELECT    Z=log10(phosphorus)
FOREACH x(14 to 20 step 0.5)
CONTOUR   VALUE=14 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=14.5 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=15 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=15.5 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=16 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=16.5 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=17 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=17.5 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=18 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=18.5 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=19 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=19.5 LINE.TYP=3 COLOR=3
CONTOUR   VALUE=20 LINE.TYP=3 COLOR=3
END
$
DEPOSITION ALUMINUM THICKNES=.75 SPACES=1
$
SELECT    Z=log10(boron) TITLE="Aluminum Deposition"
PLOT.2D   X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
```

```
   Top of the device is at y=-2.17 microns.
   Top axis is at y=-3.39 microns.

COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
COLOR      COLOR=4 ALUMINUM
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=1 COLOR=1
END
SELECT     Z=log10(phosphorus)
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=14.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=15 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=15.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=16 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=16.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=17 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=17.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=18 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=18.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=19 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=19.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=20 LINE.TYP=3 COLOR=3
END
$
ETCH       ALUMINUM START X=7 Y=0
ETCH       ALUMINUM CONTINUE X=30 Y=0
ETCH       ALUMINUM CONTINUE X=30 Y=-3
ETCH       ALUMINUM DONE X=7 Y=-3
ETCH       ALUMINUM START X=1.1 Y=0
ETCH       ALUMINUM CONTINUE X=2.9 Y=0
ETCH       ALUMINUM CONTINUE X=2.9 Y=-3
ETCH       ALUMINUM DONE X=1.1 Y=-3
$
$     Plot of final structure
$
SELECT     Z=log10(boron) TITLE="Final NMOS Power Device"
PLOT.2D    X.SIZE=0.25 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1

   Top of the device is at y=-1.41 microns.
   Top axis is at y=-2.56 microns.

COLOR       COLOR=7 SILICON
COLOR      COLOR=3 OXIDE
COLOR       COLOR=2 POLY
```

```
COLOR      COLOR=4 ALUMINUM
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=14.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=15.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=16.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=17.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=18.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=19.5 LINE.TYP=1 COLOR=1
CONTOUR    VALUE=20 LINE.TYP=1 COLOR=1
END
SELECT     Z=log10(phosphorus)
FOREACH x(14 to 20 step 0.5)
CONTOUR    VALUE=14 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=14.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=15 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=15.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=16 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=16.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=17 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=17.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=18 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=18.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=19 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=19.5 LINE.TYP=3 COLOR=3
CONTOUR    VALUE=20 LINE.TYP=3 COLOR=3
END
SELECT     Z=log10(boron) TITLE="Final Well Profile(vertical)"
PLOT.1D    X.VALUE=11 LINE.TYP=2 COLOR=2 BOTTOM=13 TOP=20 X.SIZE=0.25 +
 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4
SELECT     Z=log10(phosphorus)
PLOT.1D    X.VALUE=11 LINE.TYP=1 COLOR=1 ^AXES ^CLEAR
SELECT     Z=log10(phosphorus) TITLE="Final Source Profile(vertical)"
PLOT.1D    X.VALUE=5 LINE.TYP=1 COLOR=1 BOTTOM=13 TOP=20 X.SIZE=0.25 +
 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4
SELECT     Z=log10(boron)
PLOT.1D    X.VALUE=5 LINE.TYP=2 COLOR=2 ^AXES ^CLEAR
SELECT     Z=log10(phosphorus) TITLE="Final Drain Profile(vertical)"
PLOT.1D    X.VALUE=33 LINE.TYP=1 COLOR=1 BOTTOM=13 TOP=20 X.SIZE=0.25 +
 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4
SELECT     Z=log10(boron)
PLOT.1D    X.VALUE=33 LINE.TYP=2 COLOR=2 ^AXES ^CLEAR
SELECT     Z=log10(Phosphorus) TITLE="Final Drift Region Profile(vertical)"
PLOT.1D    X.VALUE=20 LINE.TYP=1 COLOR=1 BOTTOM=13 TOP=20 X.SIZE=0.25 +
 Y.SIZE=0.25 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4
SELECT     Z=log10(boron)
PLOT.1D    X.VALUE=20 LINE.TYP=2 COLOR=2 ^AXES ^CLEAR
$
SELECT     Z=doping
PRINT.1D   X.VALUE=32 LAYERS

 Num       Material        Top      Bottom   Thickness        Integral
   1       aluminum    -0.9411     -0.1909      0.7503      0.0000e+00
   2          oxide    -0.1909      0.4093      0.6002     -2.8208e+14
   3        silicon     0.4093     10.0000      9.5907      3.0347e+15
```

```
SELECT     Z=doping
PRINT.1D   X.VALUE=5 LAYERS

 Num       Material        Top      Bottom  Thickness        Integral
   1       aluminum    -0.8560     -0.1060     0.7500      0.0000e+00
   2          oxide    -0.1060      0.4940     0.6000      4.7418e+13
   3        silicon     0.4940      1.3834     0.8894      3.4106e+15
   4        silicon     1.3834      5.1298     3.7463     -1.0757e+12
   5        silicon     5.1298     10.0000     4.8702      2.4489e+11

SELECT     Z=doping
PRINT.1D   X.VALUE=11 LAYERS

 Num       Material        Top      Bottom  Thickness        Integral
   1          oxide    -0.8261     -0.3744     0.4517      2.6290e+13
   2          oxide    -0.3744     -0.2176     0.1567     -4.6516e+12
   3     polysilicon   -0.2176      0.3908     0.6085      6.4060e+15
   4          oxide     0.3908      0.4813     0.0905      3.2983e+12
   5          oxide     0.4813      0.4821     0.0008     -2.3951e+08
   6        silicon     0.4821      4.4579     3.9758     -6.7050e+11
   7        silicon     4.4579     10.0000     5.5421      2.7960e+11

SELECT     Z=doping
PRINT.1D   X.VALUE=25 LAYERS

 Num       Material        Top      Bottom  Thickness        Integral
   1          oxide    -0.6127      0.9012     1.5139      4.8624e+15
   2        silicon     0.9012     10.0000     9.0988      5.8418e+11

$
$SAVEFILE  OUT.FILE=MOS_DEV_S4.str SCALE=1.0
STRUCTURE OUT.FILE=MOS_MED15_S4.str SCALE=1.0 MEDICI POLY.ELE
Electrode 1: xmin    9.000 xmax   20.000 ymin    -0.793 ymax     0.396
Electrode 2: xmin    0.000 xmax    1.100 ymin    -0.204 ymax     0.494
Electrode 3: xmin    2.900 xmax    7.000 ymin    -0.106 ymax     0.494
Electrode 4: xmin   30.000 xmax   35.000 ymin    -0.653 ymax     0.407
STOP


 *** END TSUPREM-4 ***
```

Appendix B

```
TITLE
$
$ Ray Talacka
$ 7/10/94
$
$ Read in simulation mesh
$
MESH       TSUPREM4 IN.FILE=MOS_MED_S4.str RECTANGU
$
$ Set interface charges
$
INTERFACE QF=8e10
$
$ If carriers=0 is specified then gummel model is used
$
SYMBOLIC   NEWTON CARRIERS=1 ELECTRON
METHOD     CARR.MIN=1 CARR.FAC=0.5 N.DVLIM=2 NODE.ERR=0 ITLIMIT=30
$
$       Use chart for mobility calculations
$
MODELS    CONMOB
$
$ Potential Curves
$
SOLVE      V1=0 V2=0 V3=0 V4=0
SOLVE      PROJECT V1=2 V3=0 V4=25
PLOT.2D   BOUNDARY JUNC DEPL FILL SCALE
+         TITLE="POTENTIAL CONTOURS"
CONTOUR    POTENTIA MIN.VALU=0.0 NCONTOUR=25 LINE.TYP=1 COLOR=6
PLOT.2D    BOUNDARY JUNCTION DEPLETIO FILL TITLE="ELECTRON CONTOURS" T.SIZE=0.4 +
 SCALE X.SIZE=0.25 Y.SIZE=0.25
CONTOUR    ELECTRON LOGARITH FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=6
PLOT.1D    J.ELECTR X.COMPON Y.COMPON X.START=18 Y.START=0 X.END=18.5 Y.END=10 +
 HORZ.STA=0.0 TITLE="current at 18u" T.SIZE=0.4 X.SIZE=0.25 Y.SIZE=0.25
PLOT.2D    BOUNDARY JUNCTION DEPLETIO FILL TITLE="hole CONTOURS" T.SIZE=0.4 +
 SCALE X.SIZE=0.25 Y.SIZE=0.25
CONTOUR    HOLES LOGARITH FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=6
PLOT.2D    BOUNDARY JUNCTION DEPLETIO FILL TITLE="ELECTRIC FIELD CONTOURS" +
 T.SIZE=0.4 SCALE X.SIZE=0.25 Y.SIZE=0.25
CONTOUR    E.FIELD WINDOW NCONTOUR=20 FILL C.START=8 C.INCREM=1 LINE.TYP=1 +
 COLOR=6
PLOT.1D    E.FIELD X.COMPON Y.COMPON X.START=18 Y.START=-2 X.END=18.5 Y.END=10 +
 HORZ.STA=0.0 INSULATO TITLE="e field at 18u" T.SIZE=0.4 X.SIZE=0.25 +
 Y.SIZE=0.25
$
SOLVE      V1=0 V2=0 V3=0 V4=25
PLOT.2D   BOUNDARY JUNC DEPL FILL SCALE
+         TITLE="POTENTIAL CONTOURS"
CONTOUR    POTENTIA MIN.VALU=0.0 NCONTOUR=30 LINE.TYP=1 COLOR=6
PLOT.2D    BOUNDARY JUNCTION DEPLETIO FILL TITLE="ELECTRON CONTOURS" T.SIZE=0.4 +
 SCALE X.SIZE=0.25 Y.SIZE=0.25
CONTOUR    ELECTRON LOGARITH FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=6
PLOT.1D    J.ELECTR X.COMPON Y.COMPON X.START=18 Y.START=0 X.END=18.5 Y.END=10 +
 HORZ.STA=0.0 TITLE="current at 18u" T.SIZE=0.4 X.SIZE=0.25 Y.SIZE=0.25
PLOT.2D    BOUNDARY JUNCTION DEPLETIO FILL TITLE="hole CONTOURS" T.SIZE=0.4 +
 SCALE X.SIZE=0.25 Y.SIZE=0.25
CONTOUR    HOLES LOGARITH FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=6
PLOT.2D    BOUNDARY JUNCTION DEPLETIO FILL TITLE="ELECTRIC FIELD CONTOURS" +
 T.SIZE=0.4 SCALE X.SIZE=0.25 Y.SIZE=0.25
CONTOUR    E.FIELD WINDOW NCONTOUR=20 FILL C.START=8 C.INCREM=1 LINE.TYP=1 +
```

```
 COLOR=6
PLOT.1D    E.FIELD Y.COMPON X.START=20.5 Y.START=-2 X.END=21 Y.END=10 +
 HORZ.STA=0.0 TITLE="e field at 21u" T.SIZE=0.4 X.SIZE=0.25 Y.SIZE=0.25
$
STOP
```

```
**********************************************************
***                    MEDICI (TM)                     ***
***                   Version 1.2.2                    ***
***                System H (HP: HP-UX)                ***
***           Copyright (C) 1991,1992,1993             ***
***       Technology Modeling Associates, Inc.         ***
***                All Rights Reserved                 ***
**********************************************************

                      8-Nov-94 20:47:29

 Statements input from file MOS_MED.inp


  1... TITLE NMOS Power Device
  2... $
  3... $ Ray Talacka
  4... $ 7/10/94
  5... $
  6... $ Read in simulation mesh
  7... $
  8... MESH       TSUPREM4 IN.FILE=MOS_MED_S4.str RECTANGU
  9... $
 10... $ Set interface charges
 11... $
 12... INTERFACE QF=8e10
 13... $
 14... $ If carriers=0 is specified then gummel model is used
 15... $
 16... SYMBOLIC  NEWTON CARRIERS=1 ELECTRON
 17... METHOD    CARR.MIN=1 CARR.FAC=0.5 N.DVLIM=2 NODE.ERR=0 ITLIMIT=30
 18... $
 19... $ Use chart for mobility calculations
 20... $
 21... MODELS    CONMOB
 22... $
 23... $ Potential Curves
 24... $
 25... SOLVE      V1=0 V2=0 V3=0 V4=0
 26... SOLVE      PROJECT V1=2 V3=0 V4=25
 27... PLOT.2D   BOUNDARY JUNC DEPL FILL SCALE
   ... +         TITLE="POTENTIAL CONTOURS"
 28... CONTOUR    POTENTIA MIN.VALU=0.0 NCONTOUR=25 LINE.TYP=1 COLOR=6
 29... PLOT.2D    BOUNDARY JUNCTION DEPLETIO FILL TITLE="ELECTRON CONTOURS" T.SI
   ...  SCALE X.SIZE=0.25 Y.SIZE=0.25
 30... CONTOUR    ELECTRON LOGARITH FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=6
 31... PLOT.1D    J.ELECTR X.COMPON Y.COMPON X.START=18 Y.START=0 X.END=18.5 Y.E
   ...  HORZ.STA=0.0 TITLE="current at 18u" T.SIZE=0.4 X.SIZE=0.25 Y.SIZE=0.25
 32... PLOT.2D    BOUNDARY JUNCTION DEPLETIO FILL TITLE="hole CONTOURS" T.SIZE=0
   ...  SCALE X.SIZE=0.25 Y.SIZE=0.25
 33... CONTOUR    HOLES LOGARITH FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=6
 34... PLOT.2D    BOUNDARY JUNCTION DEPLETIO FILL TITLE="ELECTRIC FIELD CONTOURS
   ...  T.SIZE=0.4 SCALE X.SIZE=0.25 Y.SIZE=0.25
 35... CONTOUR    E.FIELD WINDOW NCONTOUR=20 FILL C.START=8 C.INCREM=1 LINE.TYP=
   ...  COLOR=6
```

```
 36... PLOT.1D   E.FIELD X.COMPON Y.COMPON X.START=18 Y.START=-2 X.END= B5  Y.E
   ...  HORZ.STA=0.0 INSULATO TITLE="e field at 18u" T.SIZE=0.4 X.SIZE=     +
   ...  Y.SIZE=0.25
 37... $
 38... SOLVE     V1=0 V2=0 V3=0 V4=25
 39... PLOT.2D  BOUNDARY JUNC DEPL FILL SCALE
   ... +        TITLE="POTENTIAL CONTOURS"
 40... CONTOUR   POTENTIA MIN.VALU=0.0 NCONTOUR=30 LINE.TYP=1 COLOR=6
 41... PLOT.2D   BOUNDARY JUNCTION DEPLETIO FILL TITLE="ELECTRON CONTOURS" T.SI
   ...  SCALE X.SIZE=0.25 Y.SIZE=0.25
 42... CONTOUR   ELECTRON LOGARITH FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=6
 43... PLOT.1D   J.ELECTR X.COMPON Y.COMPON X.START=18 Y.START=0 X.END=18.5 Y.E
   ...  HORZ.STA=0.0 TITLE="current at 18u" T.SIZE=0.4 X.SIZE=0.25 Y.SIZE=0.25
 44... PLOT.2D   BOUNDARY JUNCTION DEPLETIO FILL TITLE="hole CONTOURS" T.SIZE=0
   ...  SCALE X.SIZE=0.25 Y.SIZE=0.25
 45... CONTOUR   HOLES LOGARITH FILL C.START=8 C.INCREM=1 LINE.TYP=1 COLOR=6
 46... PLOT.2D   BOUNDARY JUNCTION DEPLETIO FILL TITLE="ELECTRIC FIELD CONTOURS
   ...  T.SIZE=0.4 SCALE X.SIZE=0.25 Y.SIZE=0.25
 47... CONTOUR   E.FIELD WINDOW NCONTOUR=20 FILL C.START=8 C.INCREM=1 LINE.TYP=
   ...  COLOR=6
 48... PLOT.1D   E.FIELD Y.COMPON X.START=20.5 Y.START=-2 X.END=21 Y.END=10 +
   ...  HORZ.STA=0.0 TITLE="e field at 21u" T.SIZE=0.4 X.SIZE=0.25 Y.SIZE=0.25
 49... $
 50... STOP

***************************** Program Configuration ******************************
*                                                                                *
* Programmable Device AAM  :  not authorized for use                             *
* Circuit Analysis AAM     :  not authorized for use                             *
* Lattice Temperature AAM  :  not authorized for use                             *
* Heterojunction Device AAM:  not authorized for use                             *
* Trapped Charge AAM       :      authorized for use                             *
*                                                                                *
* Maximum Nodes Available  :    3200                                             *
* Configuration Parameter  :    3200                                             *
*                                                                                *
* Approximate Number of Nodes Available for:                                     *
*   2-carrier solutions    :    3200                                             *
*   2-carrier + lat. temp. :    1856                                             *
*                                                                                *
**********************************************************************************



*****************
NMOS Power Device
*****************


Read TSUPREM-4 file from MOS_MED_S4.str

Mesh statistics (rectangular) :
    Total grid points = 2595
    Total no. of triangles = 4867
    Obtuse triangles =  168   ( 3.5%)

 Region     Material       X-min         X-max         Y-min         Y-max
   (#)        Type       (microns)     (microns)     (microns)     (microns)
---------  --------     ---------     ---------     ---------     ---------
    1       Silicon         .0000       30.0000         .4073       10.0000
```

2	Oxide	5.0000	28.0000	-1.4068	.9012
3	Oxide	1.0000	3.0000	-.1058	.4942

Electrode (#)	Number of Nodes	X-min (microns)	X-max (microns)	Y-min (microns)	Y-max (microns)
1	114	9.0000	20.0000	-.7944	.3958
2	5	.0000	1.1000	.1058	.4942
3	14	2.9000	7.0000	.1058	.4942
4	11	26.0000	30.0000	-.2285	.4073

Solution for bias:
V1 = .0000000E+00 V2 = .0000000E+00
V3 = .0000000E+00 V4 = .0000000E+00

Initial solution

norm	iter	v-error	n-error	p-error	iiter
XR	1	1.0154E+01	1.0154E+01	.0000E+00	0
XR	2	1.5029E+01	6.9104E+05	.0000E+00	0
XR	3	2.2233E+00	2.4751E+05	.0000E+00	0
XR	4	3.7105E-01	1.6325E+01	.0000E+00	0
XR	5*	1.5143E-02	1.7084E+00	.0000E+00	0
XR	6*	1.1752E-03	6.3874E+00	.0000E+00	0
XR	7*	9.2570E-05	5.8877E+01	.0000E+00	0
XR	8*	7.2975E-06	8.6023E-02	.0000E+00	0
XR	9*	5.7543E-07	8.4135E-04	.0000E+00	0
XR	10*	4.5383E-08	1.5549E-06	.0000E+00	0
XR	11	.0000E+00	9.9493E-17	.0000E+00	0

Electrode (#)	Voltage (Volts)	Flux (Coul/mic.)	I(Electron) (A/micron)	I(Hole) (A/micron)	I(Total) (A/micron)
1	.0000E+00	6.1611E-16	.0000E+00	.0000E+00	.0000E+00
2	.0000E+00	4.1036E-17	-3.0793E-36	.0000E+00	-3.0793E-36
3	.0000E+00	-6.6295E-17	-1.6667E-17	.0000E+00	-1.6667E-17
4	.0000E+00	-8.2962E-17	6.7218E-18	.0000E+00	6.7218E-18

Absolute convergence criterion met for Poisson
Absolute convergence criterion met for continuity
Total cpu time for bias point = .66 minutes
Total cpu time = .71 minutes

Solution for bias:
V1 = 2.0000000E+00 V2 = .0000000E+00
V3 = .0000000E+00 V4 = 2.5000000E+01

Warning number 51 detected in line number 26
Only 1 previous solution is present.

Warning number 57 detected in line number 26
Projection not possible, previous solution will be used
for this bias point.

Previous solution used as initial guess

norm	iter	v-error	n-error	p-error	iiter
XR	1	9.6679E+02	9.6613E+02	.0000E+00	0
XR	2	8.8940E+02	4.9910E+04	.0000E+00	0
XR	3	8.1203E+02	7.1430E+07	.0000E+00	0
XR	4	7.3466E+02	8.3547E+05	.0000E+00	0
XR	5	6.5729E+02	9.0396E+06	.0000E+00	0
XR	6	5.7993E+02	9.1934E+03	.0000E+00	0
XR	7	5.0256E+02	1.4556E+04	.0000E+00	0
XR	8	4.2521E+02	2.5226E+04	.0000E+00	0
XR	9	3.4788E+02	4.3843E+04	.0000E+00	0
XR	10	2.7050E+02	7.9470E+04	.0000E+00	0
XR	11	1.9310E+02	8.6633E+04	.0000E+00	0
XR	12	1.1573E+02	1.9250E+05	.0000E+00	0
XR	13	6.7289E+01	7.0498E+04	.0000E+00	0
XR	14	9.2504E+01	3.3171E+02	.0000E+00	0
XR	15	5.8737E+01	2.7915E+01	.0000E+00	0
XR	16	6.6648E+01	3.2779E+01	.0000E+00	0
XR	17	8.3822E+01	2.7322E+01	.0000E+00	0
XR	18	6.3671E+01	6.8417E+01	.0000E+00	0

Must try another bias point.

***** Pivot approximately zero *****
***** Repeat with smaller bias-step *****

Total cpu time for bias point = 1.39 minutes
Total cpu time = 2.10 minutes

Solution for bias:
V1 = 1.0000000E+00 V2 = .0000000E+00
V3 = .0000000E+00 V4 = 1.2500000E+01

Previous solution used as initial guess

norm	iter	v-error	n-error	p-error	iiter
XR	1	4.8324E+02	4.8271E+02	.0000E+00	0
XR	2	4.0585E+02	1.2230E+03	.0000E+00	0
XR	3	3.2849E+02	1.0206E+04	.0000E+00	0
XR	4	2.5112E+02	4.4348E+02	.0000E+00	0
XR	5	1.7375E+02	9.6683E+02	.0000E+00	0
XR	6	9.6386E+01	2.1139E+03	.0000E+00	0
XR	7	8.0918E+01	2.3466E+03	.0000E+00	0
XR	8	5.9997E+01	3.3716E+02	.0000E+00	0
XR	9	2.7094E+01	8.6084E+01	.0000E+00	0
XR	10	1.5669E+01	2.6547E+01	.0000E+00	0
XR	11	7.7363E+00	1.5576E+01	.0000E+00	0
XR	12	3.2924E+00	3.6142E+00	.0000E+00	0
XR	13	2.0216E+00	6.2738E+02	.0000E+00	0
XR	14	3.7430E-01	7.8103E+01	.0000E+00	0
XR	15	2.7211E-02	4.1641E+00	.0000E+00	0
XR	16	2.7621E-04	8.5788E+00	.0000E+00	0
XR	17*	1.5572E-06	1.5476E+02	.0000E+00	0
XR	18	.0000E+00	9.5960E-17	.0000E+00	0

Electrode (#)	Voltage (Volts)	Flux (Coul/mic.)	I(Electron) (A/micron)	I(Hole) (A/micron)	I(Total) (A/micron)
1	1.0000E+00	2.1555E-15	.0000E+00	.0000E+00	.0000E+00

2	.0000E+00	4.1036E-17	-4.7185E-21	.0000E+00	-4.7185E-21
3	.0000E+00	-6.7175E-17	-1.1125E-14	.0000E+00	-1.1125E-14
4	1.2500E+01	-8.2006E-17	1.1054E-14	.0000E+00	1.1054E-14

Absolute convergence criterion met for Poisson
Absolute convergence criterion met for continuity
Total cpu time for bias point = 1.32 minutes
Total cpu time = 3.42 minutes

Solution for bias:
V1 = 2.0000000E+00 V2 = .0000000E+00
V3 = .0000000E+00 V4 = 2.5000000E+01

Previous solution used as initial guess

norm	iter	v-error	n-error	p-error	iiter
XR	1	4.8324E+02	8.4266E+01	.0000E+00	0
XR	2	4.0585E+02	4.2256E+03	.0000E+00	0
XR	3	3.2849E+02	3.3182E+03	.0000E+00	0
XR	4	2.5112E+02	1.2105E+03	.0000E+00	0
XR	5	1.7375E+02	1.4108E+02	.0000E+00	0
XR	6	9.6386E+01	2.9803E+02	.0000E+00	0
XR	7	2.1471E+02	9.6965E+02	.0000E+00	0
XR	8	1.5790E+02	3.9994E+02	.0000E+00	0
XR	9	8.7614E+01	2.0879E+01	.0000E+00	0
XR	10	3.3103E+01	1.3424E+01	.0000E+00	0
XR	11	1.2991E+01	6.0272E+01	.0000E+00	0
XR	12	5.5345E+00	2.5885E+01	.0000E+00	0
XR	13	8.0795E-01	8.5763E+00	.0000E+00	0
XR	14	3.0041E-02	6.8035E+00	.0000E+00	0
XR	15*	9.2158E-04	3.6221E+01	.0000E+00	0
XR	16	7.0480E-06	3.1705E+00	.0000E+00	0
XR	17	.0000E+00	3.2234E-15	.0000E+00	0

Electrode (#)	Voltage (Volts)	Flux (Coul/mic.)	I(Electron) (A/micron)	I(Hole) (A/micron)	I(Total) (A/micron)
1	2.0000E+00	3.5656E-15	.0000E+00	.0000E+00	.0000E+00
2	.0000E+00	4.1036E-17	-4.8895E-21	.0000E+00	-4.8895E-21
3	.0000E+00	-6.8056E-17	-2.0275E-09	.0000E+00	-2.0275E-09
4	2.5000E+01	-8.0407E-17	2.0275E-09	.0000E+00	2.0275E-09

Absolute convergence criterion met for Poisson
Absolute convergence criterion met for continuity
Total cpu time for bias point = 1.21 minutes
Total cpu time = 4.62 minutes

Two dimensional contour plot
Input line # 28

Values plotted:

.000000E+00	1.066290E+00	2.132579E+00
3.198869E+00	4.265159E+00	5.331449E+00
6.397738E+00	7.464028E+00	8.530318E+00
9.596608E+00	1.066290E+01	1.172919E+01
1.279548E+01	1.386177E+01	1.492806E+01
1.599435E+01	1.706064E+01	1.812693E+01

```
   1.919322E+01     2.025951E+01     2.132580E+01
   2.239209E+01     2.345838E+01     2.452467E+01
   2.559096E+01


Two dimensional contour plot
Input line #       30

  Values plotted:
   2.009219E+00     4.018437E+00     6.027656E+00
   8.036875E+00     1.004609E+01     1.205531E+01
   1.406453E+01     1.607375E+01     1.808297E+01
   2.009218E+01

  Values not plotted:
  -2.009219E+00      .000000E+00     2.210140E+01

Warning number  398 detected in line number  31
More than one coordinate component has been specified.  Plotting
the magnitude of the quantity instead.


Two dimensional contour plot
Input line #       33

  Values plotted:
     .000000E+00     1.913039E+00     3.826078E+00
   5.739117E+00     7.652156E+00     9.565195E+00
   1.147823E+01     1.339127E+01     1.530431E+01
   1.721735E+01     1.913039E+01

  Values not plotted:
  -1.913039E+00     2.104343E+01


Two dimensional contour plot
Input line #       35

  Values plotted:
   1.025957E+04     2.051913E+04     3.077870E+04
   4.103827E+04     5.129783E+04     6.155740E+04
   7.181697E+04     8.207653E+04     9.233609E+04
   1.025957E+05     1.128552E+05     1.231148E+05
   1.333743E+05     1.436339E+05     1.538935E+05
   1.641530E+05     1.744126E+05     1.846722E+05
   1.949317E+05

  Values not plotted:
  -1.025957E+04      .000000E+00     2.051913E+05

Warning number  398 detected in line number  36
More than one coordinate component has been specified.  Plotting
the magnitude of the quantity instead.


Solution for bias:
  V1  =    .0000000E+00      V2  =    .0000000E+00
  V3  =    .0000000E+00      V4  =  2.5000000E+01
```

Previous solution used as initial guess

norm	iter	v-error	n-error	p-error	iiter
XR	1	6.5166E+01	3.0197E+01	.0000E+00	0
XR	2	1.5637E+01	1.0440E+07	.0000E+00	0
XR	3	4.6003E+00	7.8023E+04	.0000E+00	0
XR	4	1.0000E+00	7.9288E+00	.0000E+00	0
XR	5	1.0000E+00	2.5648E+02	.0000E+00	0
XR	6	1.0000E+00	4.8105E+01	.0000E+00	0
XR	7	1.0000E+00	1.0003E+02	.0000E+00	0
XR	8	1.0000E+00	4.4409E+01	.0000E+00	0
XR	9	1.0000E+00	2.0151E+01	.0000E+00	0
XR	10	1.0000E+00	1.9179E+01	.0000E+00	0
XR	11	1.0000E+00	3.5958E+02	.0000E+00	0
XR	12	1.0000E+00	9.2656E+02	.0000E+00	0
XR	13	1.0000E+00	9.3956E+00	.0000E+00	0
XR	14	1.0000E+00	1.7714E+01	.0000E+00	0
XR	15	1.0000E+00	1.8694E+02	.0000E+00	0
XR	16	1.0000E+00	2.2059E+01	.0000E+00	0
XR	17	1.0000E+00	2.9676E+01	.0000E+00	0
XR	18	1.0000E+00	1.9062E+01	.0000E+00	0
XR	19	1.0000E+00	1.9783E+01	.0000E+00	0
XR	20	1.0000E+00	1.2819E+01	.0000E+00	0
XR	21	1.0000E+00	6.6503E+00	.0000E+00	0
XR	22	1.0000E+00	3.4217E+00	.0000E+00	0
XR	23	1.0000E+00	1.6586E+01	.0000E+00	0
XR	24	1.0000E+00	1.0024E+00	.0000E+00	0
XR	25	1.0000E+00	1.0022E+00	.0000E+00	0
XR	26	9.9998E-01	1.0017E+00	.0000E+00	0
XR	27	9.9994E-01	1.0014E+00	.0000E+00	0
XR	28	9.9979E-01	1.0010E+00	.0000E+00	0
XR	29	9.9932E-01	5.4244E-03	.0000E+00	0
XR	30	9.9781E-01	4.0833E-03	.0000E+00	0

***** Convergence problem *****
***** Repeat with smaller bias-step *****

Total cpu time for bias point = 2.19 minutes
Total cpu time = 7.21 minutes

Solution for bias:

V1 = 1.0000000E+00 V2 = .0000000E+00
V3 = .0000000E+00 V4 = 2.5000000E+01

Previous solution used as initial guess

norm	iter	v-error	n-error	p-error	iiter
XR	1	3.2583E+01	1.5099E+01	.0000E+00	0
XR	2	6.7347E+00	1.1857E+05	.0000E+00	0
XR	3	2.2747E+00	3.8610E+01	.0000E+00	0
XR	4	9.9998E-01	7.3593E+00	.0000E+00	0
XR	5	9.9991E-01	1.1662E+04	.0000E+00	0
XR	6	9.9969E-01	5.8712E+03	.0000E+00	0
XR	7	9.9892E-01	5.0911E+03	.0000E+00	0
XR	8	9.9630E-01	2.8784E+03	.0000E+00	0
XR	9	9.8773E-01	4.1229E+01	.0000E+00	0
XR	10	9.6073E-01	2.9333E+00	.0000E+00	0

XR	11	8.8005E-01	3.1624E+00	.0000E+00	0	
XR	12	6.7039E-01	3.4540E-01	.0000E+00	0	B11
XR	13	3.0905E-01	5.5826E-02	.0000E+00	0	
XR	14	4.7405E-02	1.0716E-04	.0000E+00	0	
XR	15*	8.7660E-04	4.9911E-13	.0000E+00	0	
XR	16*	3.2302E-05	1.6553E-14	.0000E+00	0	
XR	17*	1.1995E-06	6.3493E-16	.0000E+00	0	
XR	18	.0000E+00	9.9451E-17	.0000E+00	0	

Electrode (#)	Voltage (Volts)	Flux (Coul/mic.)	I(Electron) (A/micron)	I(Hole) (A/micron)	I(Total) (A/micron)
1	1.0000E+00	1.2928E-15	.0000E+00	.0000E+00	.0000E+00
2	.0000E+00	4.1036E-17	-4.8894E-21	.0000E+00	-4.8894E-21
3	.0000E+00	-6.7175E-17	-1.1948E-14	.0000E+00	1.1948E-14
4	2.5000E+01	-8.0246E-17	1.1987E-14	.0000E+00	1.1987E-14

Absolute convergence criterion met for Poisson
Absolute convergence criterion met for continuity
Total cpu time for bias point = 1.20 minutes
Total cpu time = 8.41 minutes

Solution for bias:
V1 = .0000000E+00 V2 = .0000000E+00
V3 = .0000000E+00 V4 = 2.5000000E+01

Projection used to find initial guess

norm	iter	v-error	n-error	p-error	iiter
XR	1	4.0340E+00	7.7901E+02	.0000E+00	0
XR	2	1.0958E+00	4.4181E+00	.0000E+00	0
XR	3	1.0000E+00	8.7243E-01	.0000E+00	0
XR	4	1.0000E+00	5.6111E-01	.0000E+00	0
XR	5	1.0000E+00	1.9482E-02	.0000E+00	0
XR	6	1.0000E+00	1.7663E-02	.0000E+00	0
XR	7	1.0000E+00	1.6606E-02	.0000E+00	0
XR	8	1.0000E+00	1.5932E-02	.0000E+00	0
XR	9	1.0000E+00	1.5052E-02	.0000E+00	0
XR	10	9.9999E-01	1.4428E-02	.0000E+00	0
XR	11	9.9996E-01	1.4205E-02	.0000E+00	0
XR	12	9.9985E-01	1.3716E-02	.0000E+00	0
XR	13	9.9949E-01	1.2041E-02	.0000E+00	0
XR	14	9.9829E-01	9.3117E-03	.0000E+00	0
XR	15	9.9436E-01	5.7096E-03	.0000E+00	0
XR	16	9.8196E-01	2.6575E-03	.0000E+00	0
XR	17	9.4481E-01	1.2521E-03	.0000E+00	0
XR	18	8.4258E-01	1.0749E-03	.0000E+00	0
XR	19	6.0935E-01	8.4536E-04	.0000E+00	0
XR	20	2.6211E-01	3.2771E-04	.0000E+00	0
XR	21	3.7434E-02	3.0570E-05	.0000E+00	0
XR	22*	6.3231E-04	3.0777E-13	.0000E+00	0
XR	23*	2.1406E-05	1.0521E-14	.0000E+00	0
XR	24*	7.3081E-07	4.3050E-16	.0000E+00	0
XR	25	.0000E+00	9.9287E-17	.0000E+00	0

Electrode (#)	Voltage (Volts)	Flux (Coul/mic.)	I(Electron) (A/micron)	I(Hole) (A/micron)	I(Total) (A/micron)

1	.0000E+00	-1.1868E-15	.0000E+00	.0000E+00	.0000E+00
2	.0000E+00	4.1036E-17	-4.8892E-21	.0000E+00	-4.8892E-21
3	.0000E+00	-6.6295E-17	-1.7477E-16	.0000E+00	1.7477E-16
4	2.5000E+01	-8.0083E-17	-2.5100E-16	.0000E+00	-2.5100E-16

Absolute convergence criterion met for Poisson
Absolute convergence criterion met for continuity
Total cpu time for bias point = 1.70 minutes
Total cpu time = 10.11 minutes

B12

Two dimensional contour plot
Input line # 40

Values plotted:

.000000E+00	8.824466E-01	1.764893E+00
2.647340E+00	3.529787E+00	4.412233E+00
5.294680E+00	6.177127E+00	7.059574E+00
7.942020E+00	8.824467E+00	9.706913E+00
1.058936E+01	1.147181E+01	1.235425E+01
1.323670E+01	1.411914E+01	1.500159E+01
1.588404E+01	1.676648E+01	1.764893E+01
1.853138E+01	1.941382E+01	2.029627E+01
2.117871E+01	2.206116E+01	2.294361E+01
2.382605E+01	2.470850E+01	2.559095E+01

Two dimensional contour plot
Input line # 42

Values plotted:

2.009219E+00	4.018437E+00	6.027656E+00
8.036875E+00	1.004609E+01	1.205531E+01
1.406453E+01	1.607375E+01	1.808297E+01
2.009218E+01		

Values not plotted:

-2.009219E+00	.000000E+00	2.210140E+01

Warning number 398 detected in line number 43
More than one coordinate component has been specified. Plotting the magnitude of the quantity instead.

Two dimensional contour plot
Input line # 45

Values plotted:

.000000E+00	1.913039E+00	3.826078E+00
5.739117E+00	7.652156E+00	9.565195E+00
1.147823E+01	1.339127E+01	1.530431E+01
1.721735E+01	1.913039E+01	

Values not plotted:

-1.913039E+00	2.104343E+01

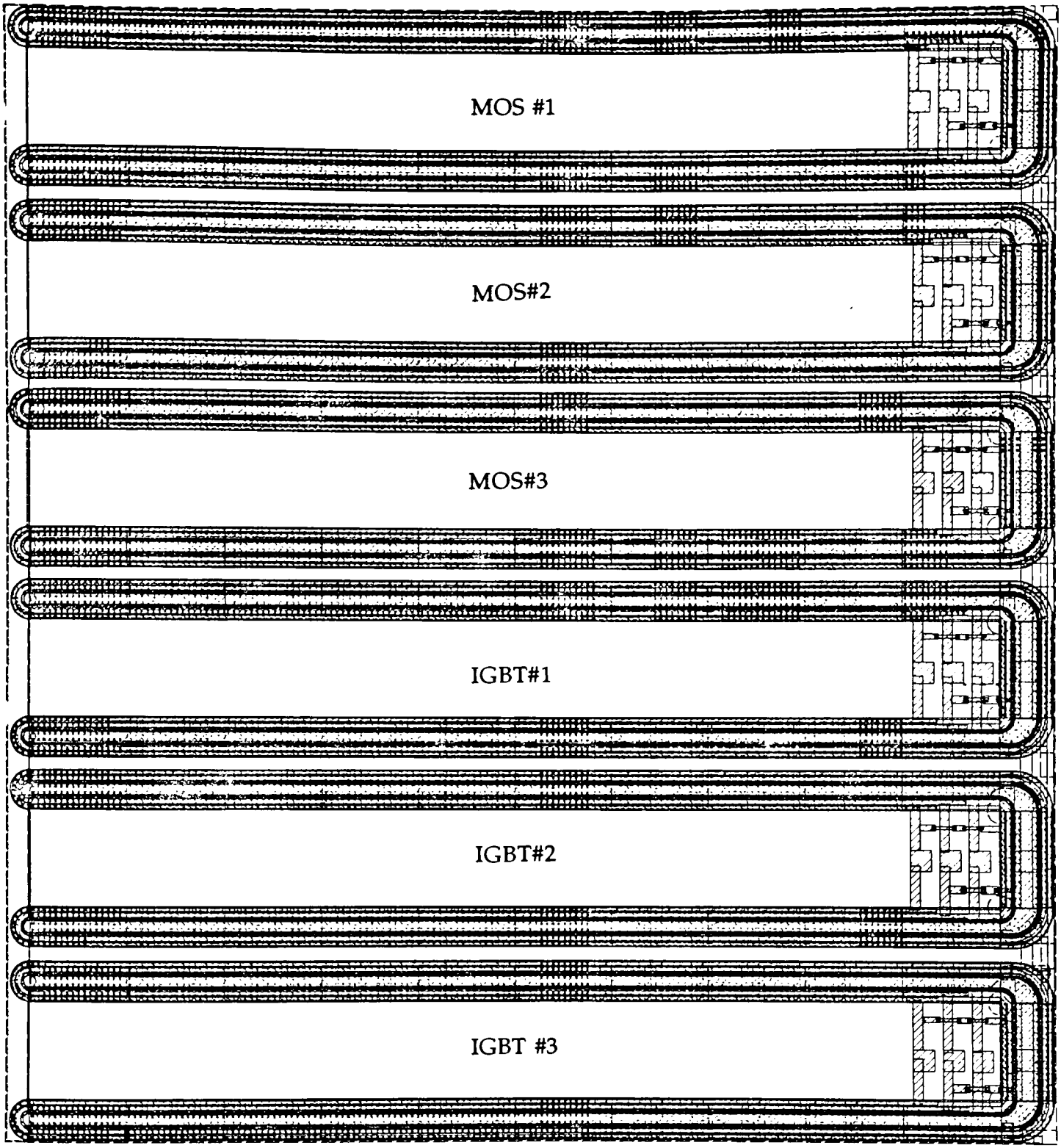
Two dimensional contour plot
Input line # 47

```
 Values plotted:
  1.105759E+04    2.211518E+04    3.317277E+04
  4.423036E+04    5.528795E+04    6.634554E+04
  7.740313E+04    8.846072E+04    9.951831E+04
  1.105759E+05    1.216335E+05    1.326911E+05
  1.437487E+05    1.548063E+05    1.658639E+05
  1.769215E+05    1.879791E+05    1.990367E+05
  2.100943E+05

 Values not plotted:
 -1.105759E+04     .000000E+00    2.211518E+05


*** END MEDICI ***

TOTAL CPU TIME =    10.49 minutes
```

Appendix C

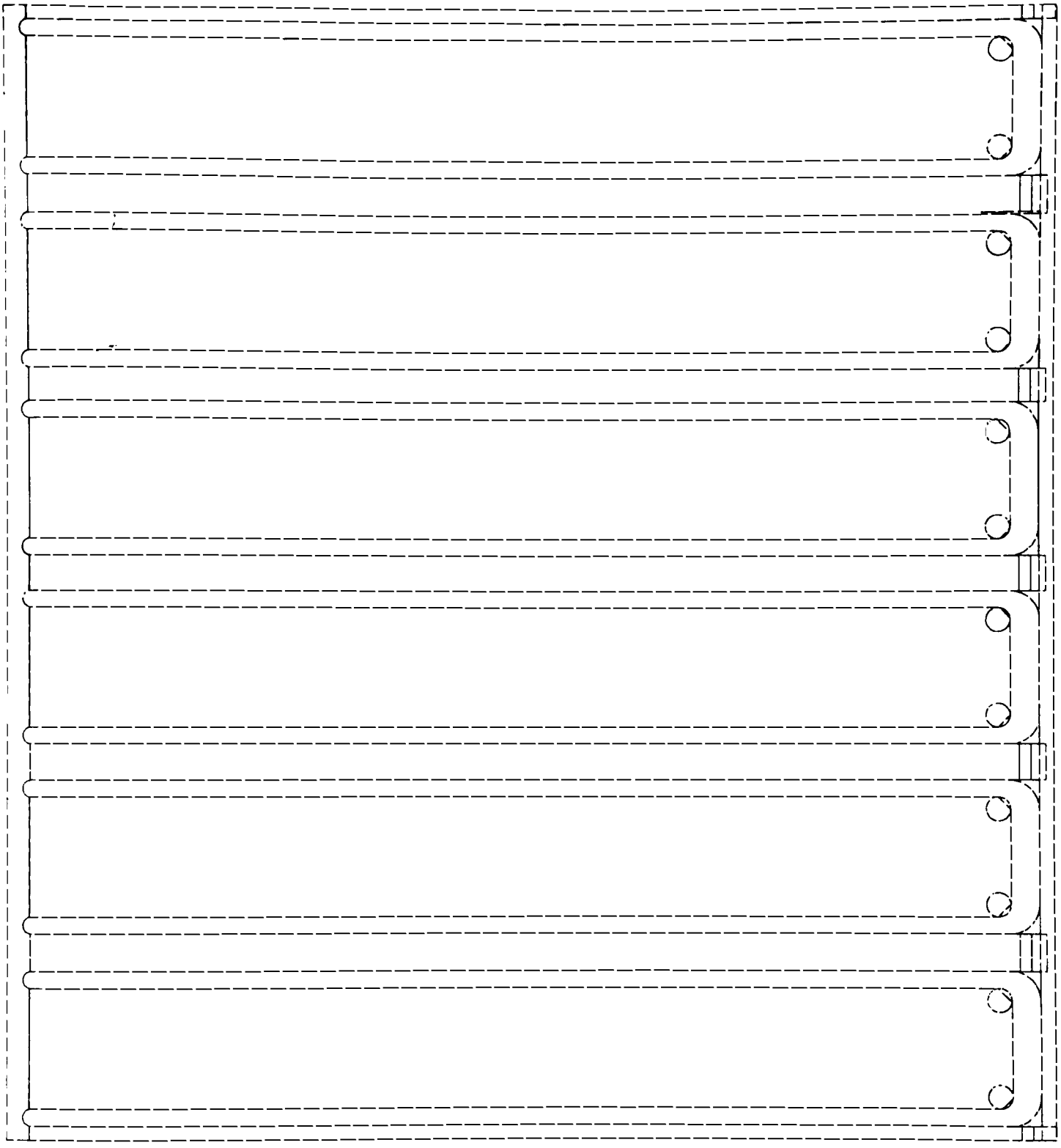
This appendix contains the IC Station design layers used to produce the masks need to fabricate the chip. The following table shows the differences in the six devices designed.

	Field Plate Length	Field Oxide Length	Drift Region Length
MOS #1	3	7	10
MOS #2	4	6	10
MOS #3	5	5	10
IGBT #1	3	7	10
IGBT #2	4	6	10
IGBT #3	5	5	10



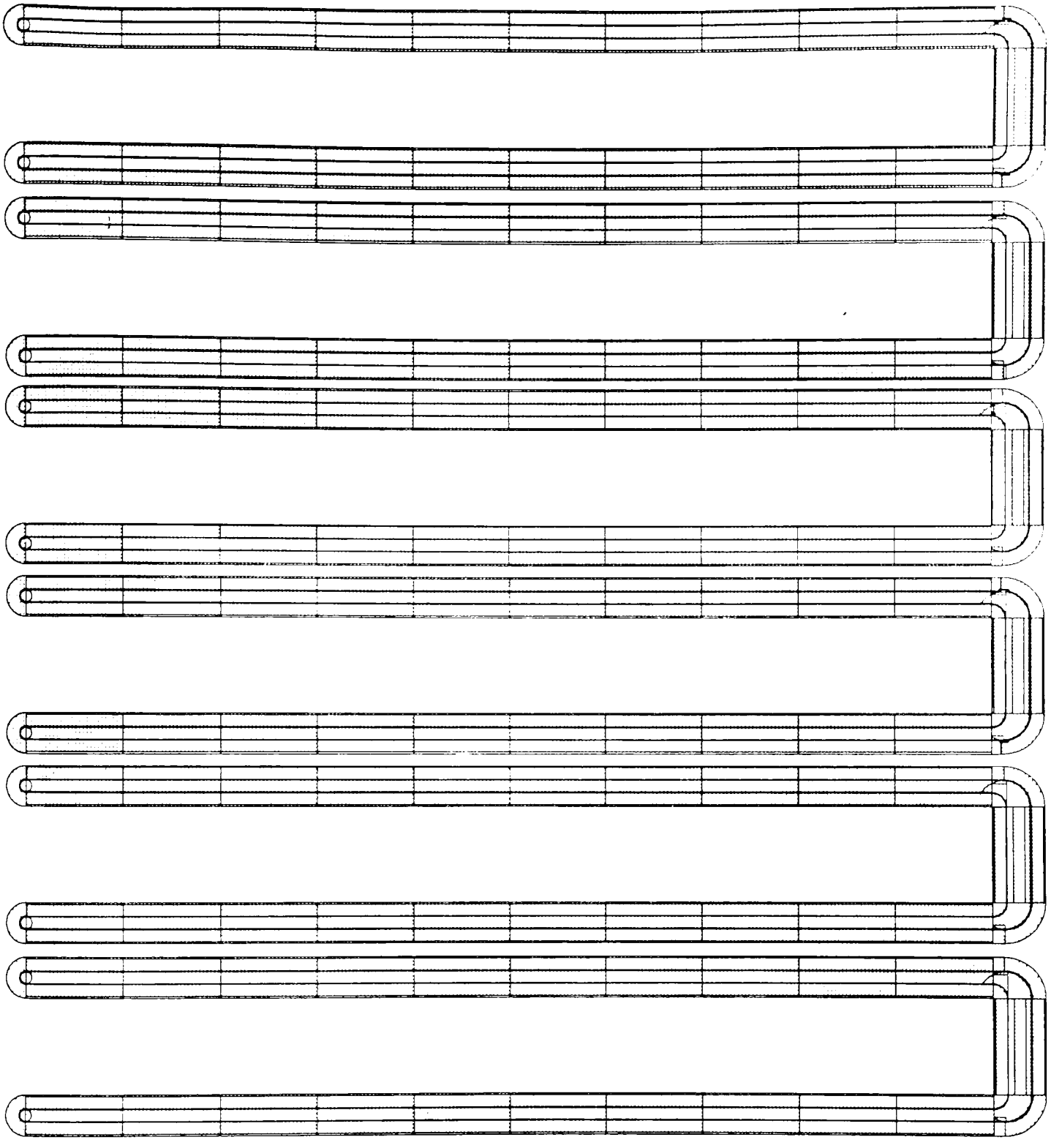
All IC Station layers

Fig C1



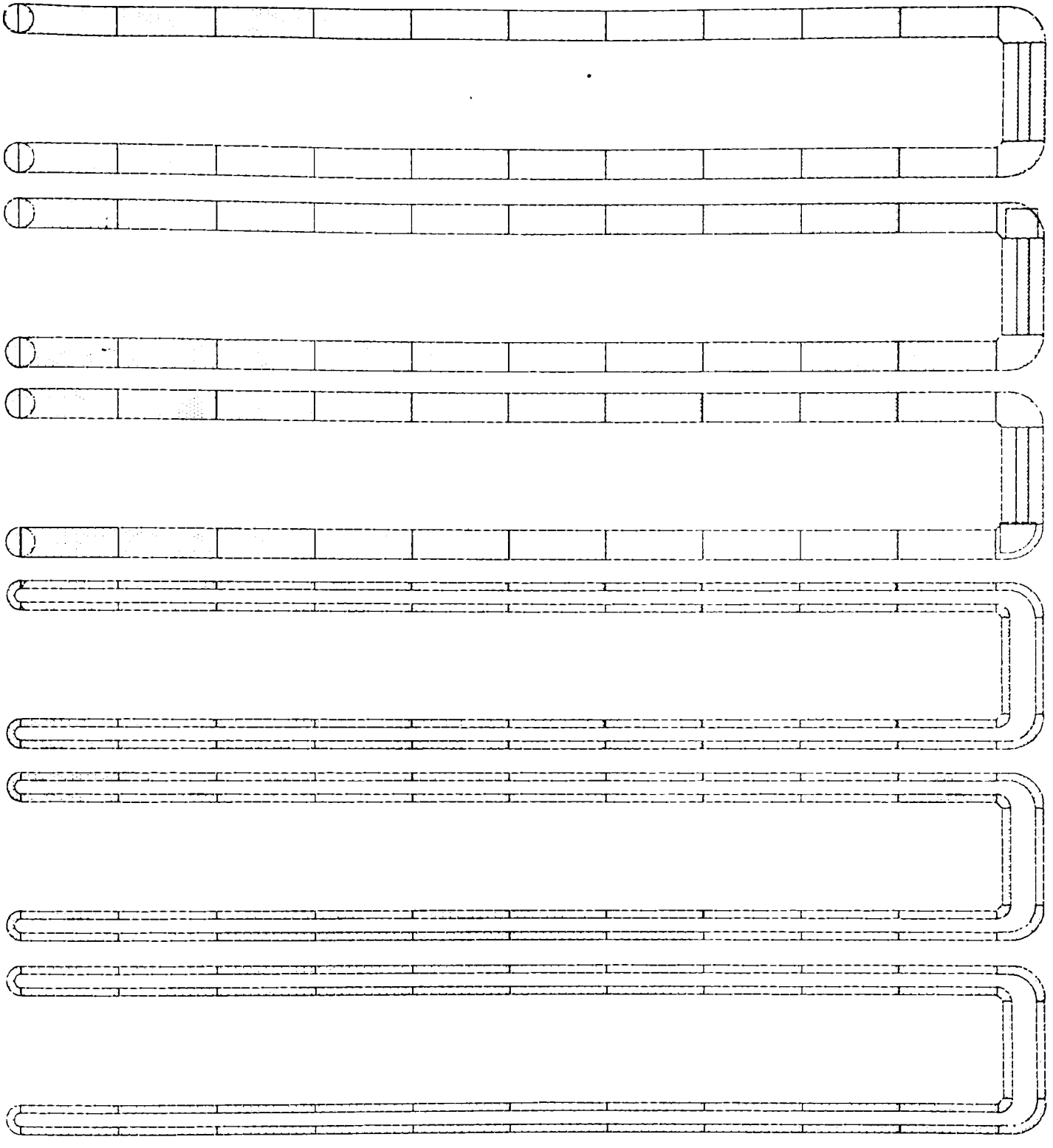
P well, IC Station layer

Fig C2



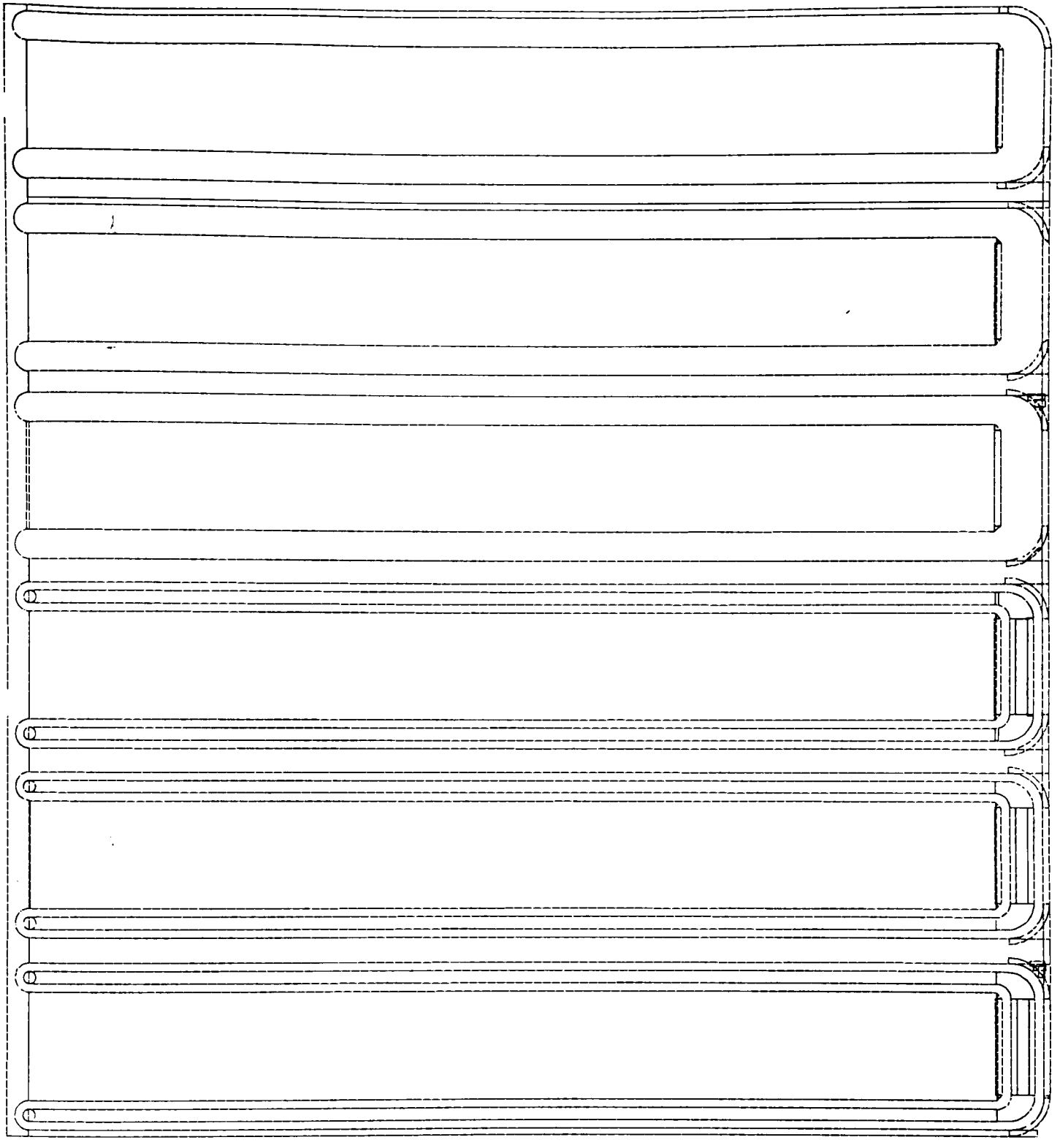
Active, IC Station layer

Fig C3



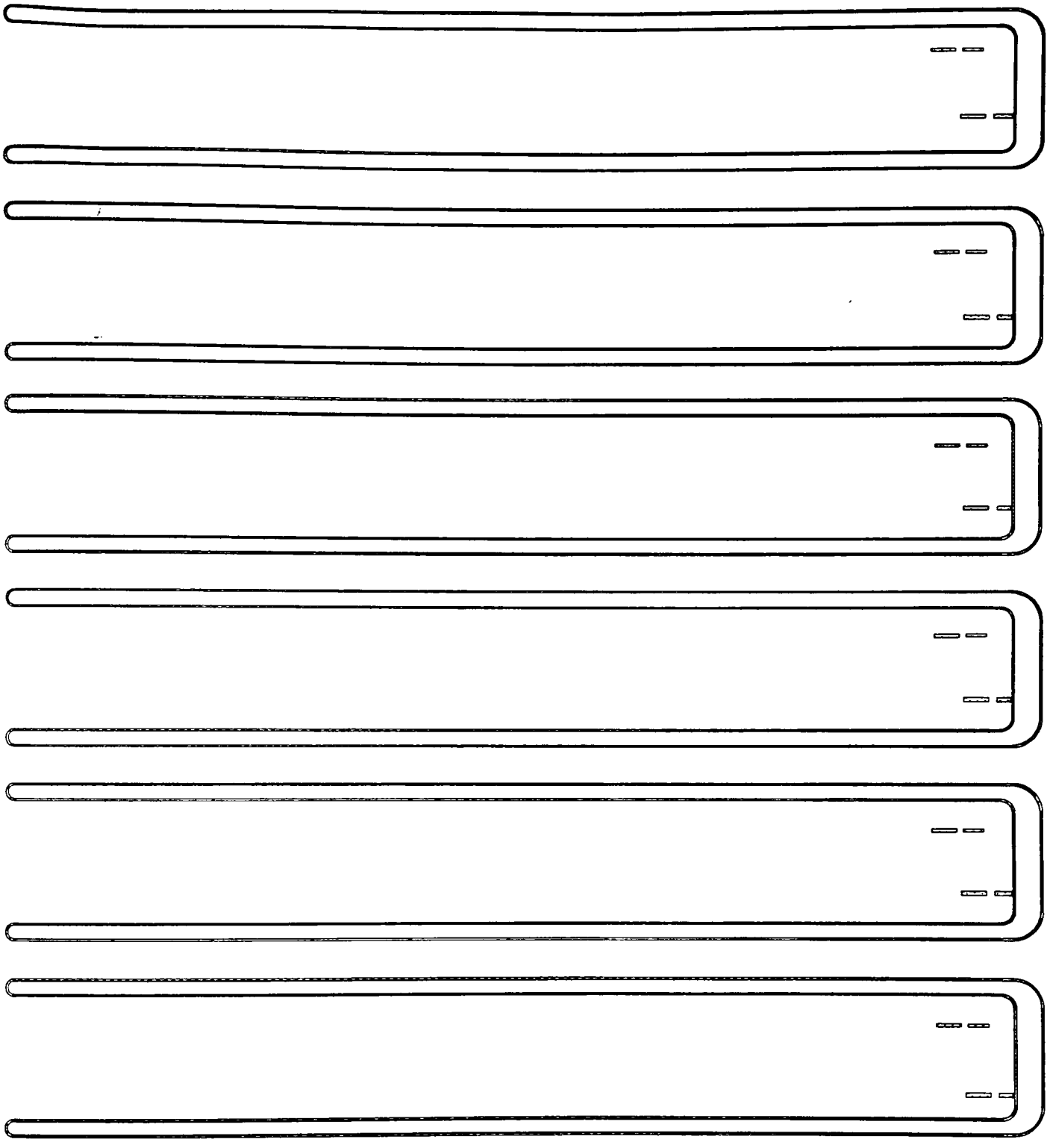
N+, IC Station layer

Fig C4



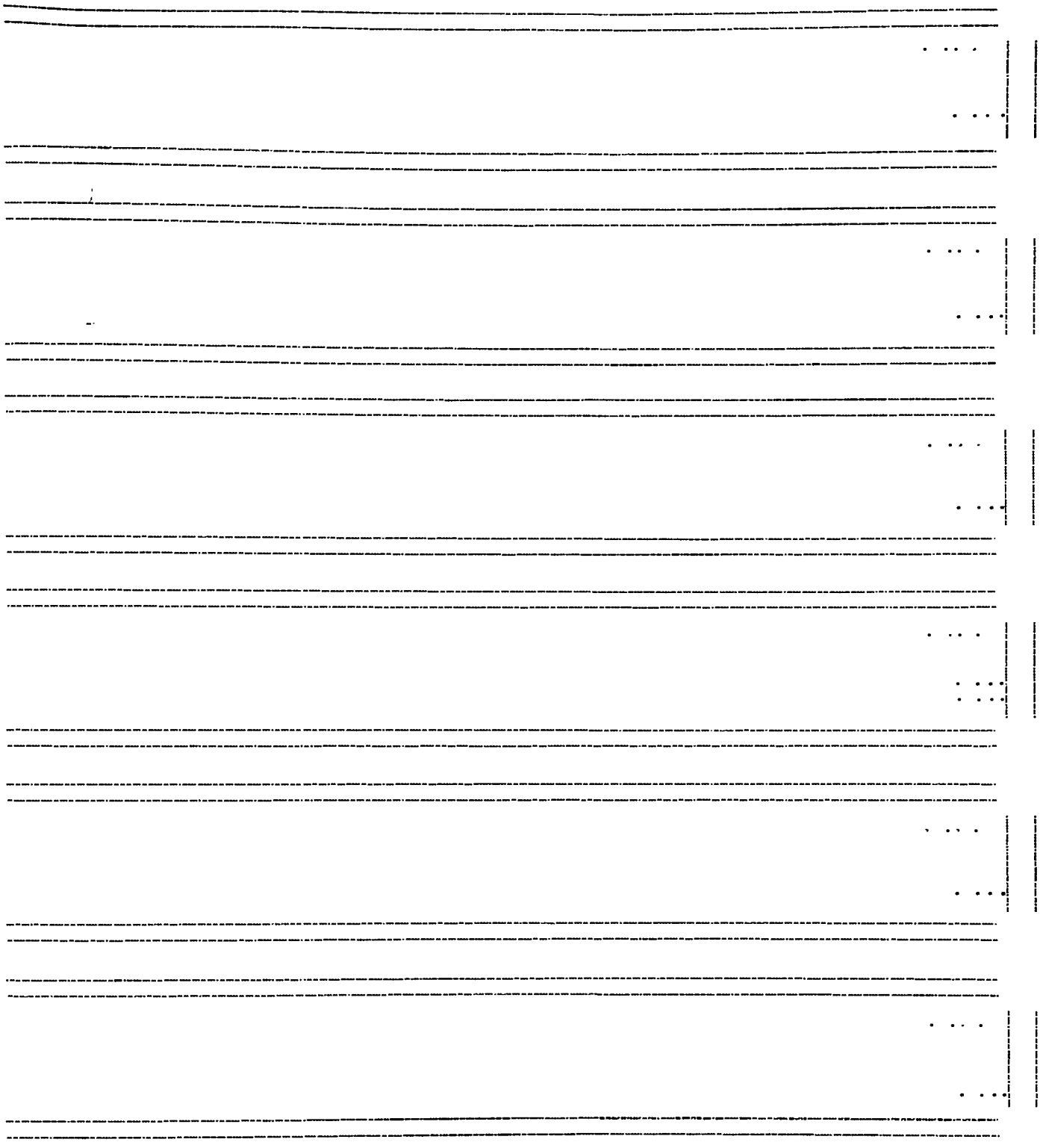
P+, IC Station layer

Fig C5



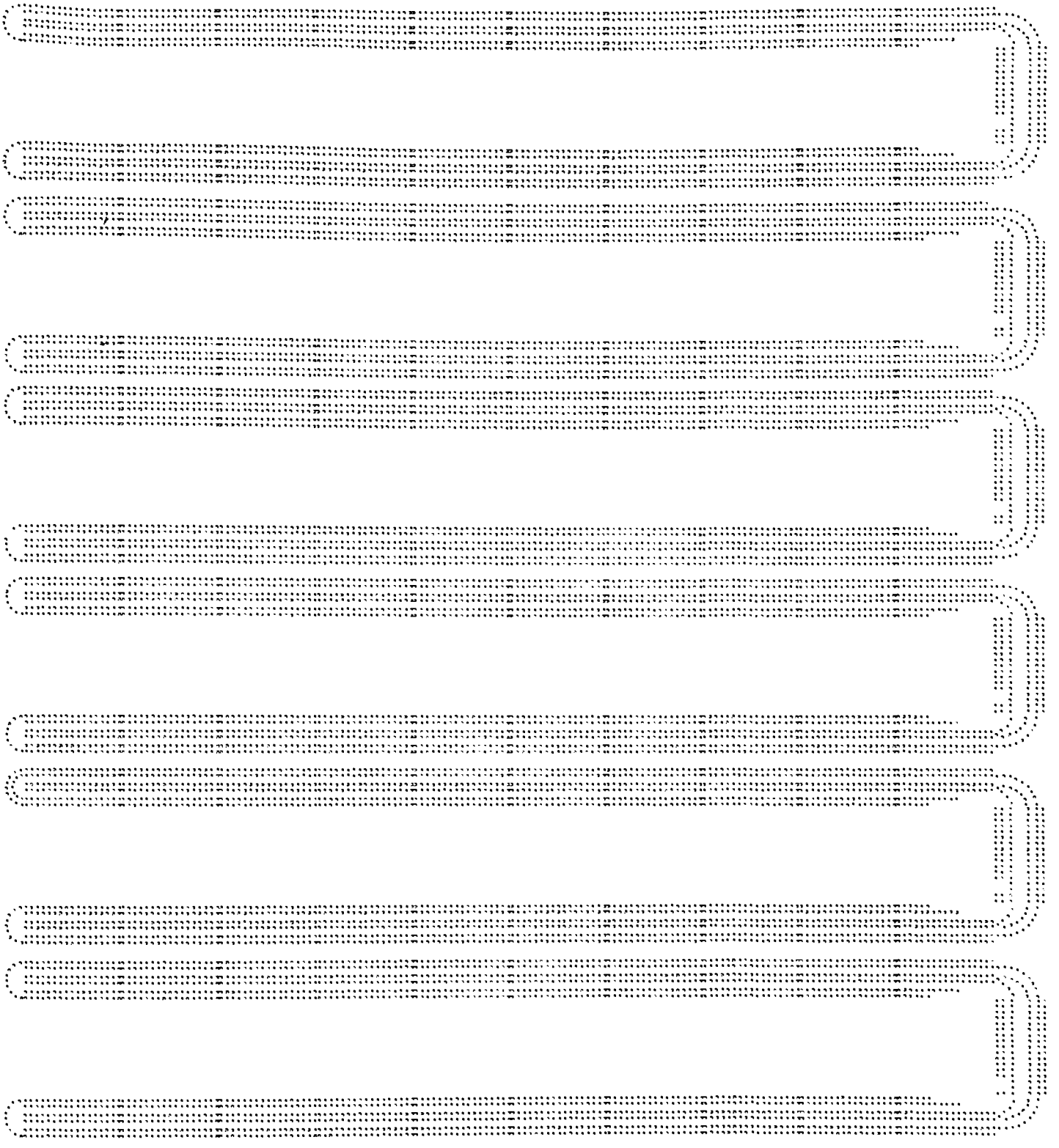
Poly, IC Station layer

Fig C6



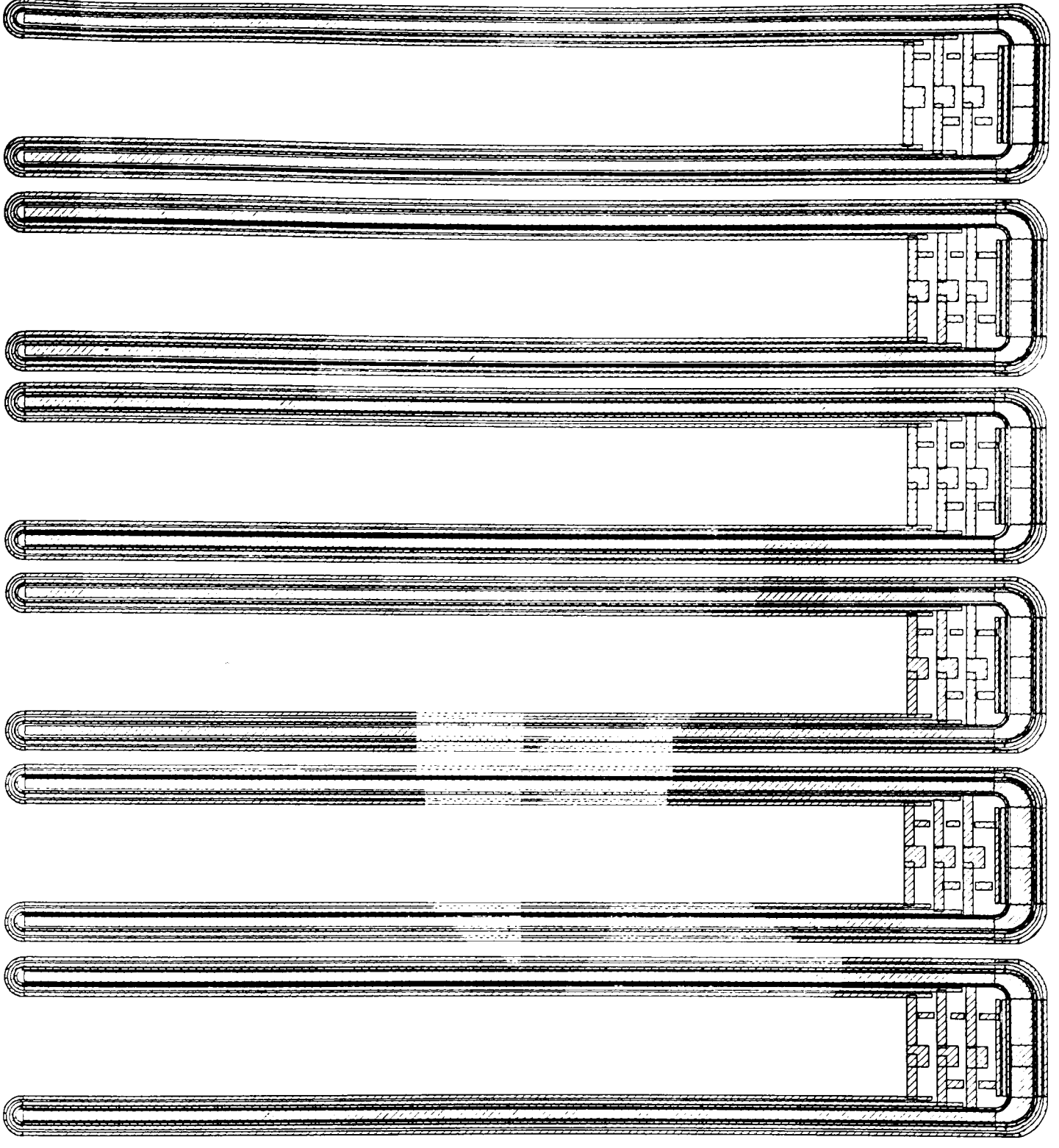
Contact to ploy, IC Station layer

Fig C7



Contact to active, IC Station layer

Fig C8



Metal, IC Station layer

Fig C9

Appendix D

4 Point Probe

	ρ (Ωcm)
W 1	8.2
W 2	7.1
W 3	8.0
W 4	7.9
W 5	7.0

-Modified RCA Clean

	Before	After
B1	249	39
B2	131	46
B3	41	23
B4	49	63

Alignment Oxide

Temp = 1100 C
Time = 35 min
Tox = 4400å

Lithography

Stepper job name = [10,20]NEWCMOS.FAC\1T,1d

Oxide Etch

Time = 6 min

Modified RCA Clean

	Before	After
B1	76	61
B2	58	54
B3	23	11
B4	69	18

Ion Implant

Vac = 15 KeV
DIED = 19
AMU = 12.8

Drive-In

Temp = 1100 C
Time = 240 min, Dry O2
Time = 960 min, N2
Tox = 3500å

4 Point Probe

	ρ (Ωcm)
C2	1.3

Grove

Xj = 5.4μm

Pad Oxide

Temp = 1000 å Wet O2
Time = 50 min
Tox = 1050å

Nitride Deposition

Time = 23 min
Tni = 1300å

Nitride Etch Rate

Etch = 1340å/min

Oxide Etch

Time = 1.5 min

Ion Implant

Vac = 65 KeV
DIED = 59
AMU = 12.6

Modified RCA Clean

	Before	After
B1	194	25
B2	102	7
B3	62	3
B4	313	31

WAFER #1 was broken during the modified RCA clean

Field Oxide

Temp = 1100 C Wet O2
Time = 210 min
Tox = 11,250å

Nitride Etch

BOE = 0.5 min
Etch = 1340 å/min

Oxide Etch

Time = 1.5 min

Modified RCA Clean

	Before	After
B1	53	33
B2	51	22
B3	51	20
B4	45	23

KOOI Oxide

Temp = 1000 C Wet O2
Time = 45 min
Tox = 800 å

Ion Implant

Vac = 25 KeV
DIED = 29
AMU = 12.5

Lithography masking

Ion Implant

Vac = 25 KeV
DIED = 29
AMU = 12.5

Oxide Etch

Time = 1.5 min

Modified RCA Clean

	Before	After
B1	370	74
B2	483	51
B3	41	14
B4	762	41

Gate Oxide

W1,W2	Temp = 1100 C	Ramp up and down in DRY O2
	Time = 35 min	
	Tox = 990 å	
W3,W4,W5	Temp = 1100 C	Dry O2
	Time = 35 min	
	Tox = 677	

Control wafer C4 Broken, could not check junction depth or resistance at this point

CVD Poly

Time = 23 min
Tpoly = 5300 å

Spin on Dopant

Spin = 3000 rpm
Time = 30 sec
Bake = 250 C for 25 min
900 C for 10 min

Photolith

Lift off problem encountered

Poly Etch

Etch = 2444.4 A/min

Ion Implant

Vac = 85 KeV
DIED = 91
AMU = 12.7

Resist strip required 30 min in the ASHER, The wet strip was not sufficient to remove the implant hardened resist.

Ion Implant

Vac = 90 KeV ONLY P31 Implant, all others are B11
DIED = 88
AMU = 31.9

Resist strip required 30 min in the ASHER, The wet strip was not sufficient to remove the implant hardened resist.

Grove

C6 Xj = 1.2 μm
C7 Xj = .8 μm

4 Point Probe

C6 ρ = .01
C7 ρ = .008

Spin on Glass

Spin = 3000 rpm
Time = 30 sec
Bake = 250 C for 25 min
900 C for 10 min

Modified RCA Clean

	Before	After
B1	1295	456
B2	573	367
B3	448	422
B4	389	219

Al Sputter

Time = 18 min
Tal = 0.75 μm

Al Etch

Etch = .035 μm/min
Time = 3 min

Sinter

Temp = 450 C Forming Gas
Time = 20 min

Spin on Glass

Spin = 3000 rpm
Time = 30 sec
Bake = 250 C for 25 min
900 C for 10 min
Needed to repeat this step three times to obtain oxide thickness

Oxide Etch

Time = 1.75 min in special oxide on Al etch solution